EXAR

XR-212AS MODEM DESIGN BOOKLET

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I. THE BELL 212A MODEM

INTRODUCTION

The Bell 212A modem is a full-duplex modem designed for use on the public switched telephone network. Since the telephone network presents a bandpass characteristic to its users, the Bell 212A must operate under its constraints. The most critical of these constraints is the 300 Hz to 3 KHz bandpass cut-off frequencies of the phone line(see Appendix A). The purpose of the modem is to translate digital signals into analog signals and transmit these analog signals over the phone line while simultaneously receiving similarly translated analog signals from another modem. These received signals are finally demodulated to recover digital data, thus completing the modulation/demodulation process. This process is illustrated in Figure 1.
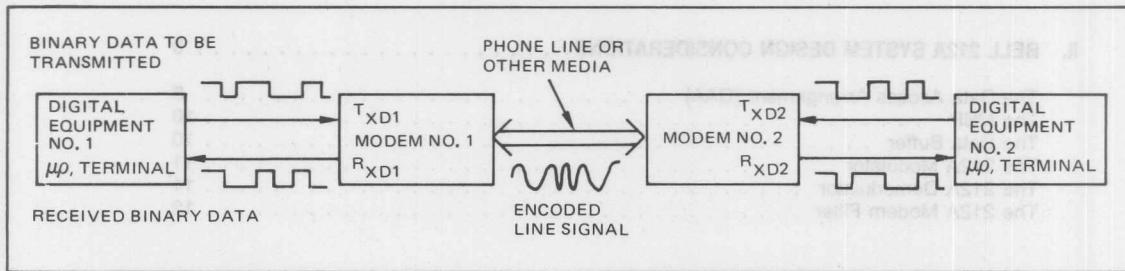

Figure 1. Data Communication via Modem

CONVENTIONS

The modem initiating communications between a pair of modems is known as the Originate modem and the receive modem is the Answer modem. The translation of digital signals to analog signals takes two forms in the Bell 212A modem. The high speed mode, which generates 1200 bits per second (BPS), uses phase shift keyed (PSK) modulation. Bell 212A differential PSK or DPSK modulation utilizes constant frequency carrier phase shifting to represent two bits (a dibit) of data (see Figure 2). This implies that the carrier of the high speed mode undergoes 600 changes per second or runs at 600 baud. The Originate modem generates a transmit carrier of 1200 Hz, and the Answer modem a transmit carrier of 2400 Hz. The low speed mode produces 300 BPS, and uses frequency shift keyed (FSK) modulation. FSK modulation represents each bit with a specific frequency. The higher frequency represents a digital "one" and is known as a mark while the lower frequency represents a digital "zero" and is known as a space. The Originate mode uses 1270 Hz and 1070 Hz for mark and space, and the Answer mode uses 2225 Hz and 2025 Hz for mark and space (see Figure 3).
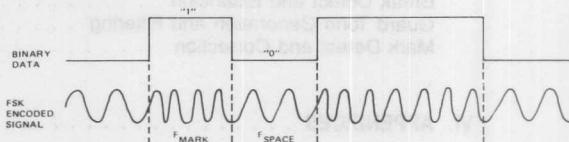
Figure 3. Representation of a FSK Signal

Bell 212A type modems utilize synchronous and character-asynchronous data formats in the high speed mode (1200 BPS). In the asynchronous mode, character lengths of 9 and 10 bits are standard for the Bell 212A. Each of these character lengths consists of one start bit and one stop bit , the difference being a function of word length: 7 or 8 bits.

The synchronous mode relies on synchronization of data with a transmit clock, and is more efficient than asynchronous communication by 2 bits (the start and stop bits, which do not appear in synchronous communication) per character. It should be noted however that asynchronous operation is by far most popular for 212A modems. The low speed (300 BPS) mode operates in the bit-asynchronous mode.

STANDARD	BELL 212A/V.22				BELL 201/V.26			
Phase Shift	0°	+90°	–90°	+180°	45°	135°	225°	315°
Dibit Value	01	00	11	10	00	01	11	10

**Figure 2. Representation of a PSK Signal**

CHARACTERISTICS

In the high speed (1200 BPS) mode, the occurrence of a series of consecutive 0° phase shifts must be presented. If no provisions were made for this possible sequence (a series of 01 dibits), the demodulator would loose the timing information necessary to process the incoming signal.

In order to compensate for the possbility of data with consecutive 0° phase shifts, the PSK modulator "scrambles" the data. The process of scrambling data involves the exclusive ORing of previous data bits with current data bits via shift registers and logic as shown in Figure 4. The scrambler is characterized by the equation

$$T_{XDI} \, S_{CR} = \overline{T_{XDI}} \oplus (T_{XDI} - 14 \oplus T_{XDI} - 17)$$
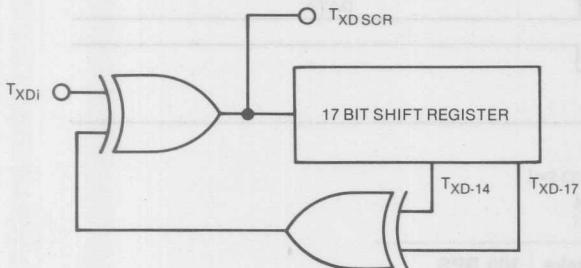

Figure 4. Scrambler

Once the scrambled data has been received and demodulated, it must be descrambled. The descrambler is shown in Figure 5 and is characterized by the equation

$$R_{XDI} \, D_{ES} = R_{XDI} \oplus (R_{XDI} - 14 \oplus R_{XDI} - 17)$$
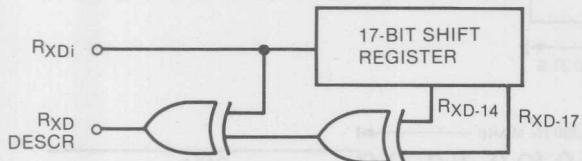

Figure 5. Descrambler

Please note that this PSK modulation/demodulation technique will produce 3 bit errors for each actual bit error when the modem is operated asynchronously. This is a direct result of the scrambler/descrambler process.

Since the intended medium of data transmission is the public switched telephone network, all Bell 212A modems exhibit similar line interface characteristics. These characteristics are dictated by part 68 of the FCC Rules. The characteristics of prime importance are an AC off-hook impedance of 600 ohms and a DC off-hook impedance of less than 200 ohms, 2 second billing delay before data transmission on auto-answer modems, attentuated signal levels outside the 300 Hz to 3 KHz of the phone line passband, transient protection, other energy level restrictions, and modem/phone line connector type. These characteristics are implemented in the Data Access Arrangement (DAA) subsystem.

The typical Bell 212A modem also utilizes the EIA connector pin assignments (modified RS232) for serial interface to the Data Terminal Equipment (DTE). These pin assignments can be found in Appendix B. Bell 212A modems which interface with a host processor over a parallel bus can provide the information as necessary. Many Bell 212A modems do not implement all of the EIA signals.

Since Bell 212A modems can operate at two speeds (300/1200 BPS), it is necessary first to determine if one 212A is talking to another 212A, then to determine what speed the Originate modem is in so that the Answer modem can adjust. This process is called the Handshake.

Once the Answer modem has detected a ring and taken the line off-hook, a two second billing delay ensues. On conclusion of the billing delay, the Answer modem transmits a 2225 Hz Answer tone to the Originate modem to signal connection. The Originate modem then responds with a mark at the speed at which it is set.

In the low speed mode, the Answer modem sends data on detection of the the 1270 Hz mark from the Originate modem, and the Originate modem transmits data on conclusion of the 1270 Hz mark. The low speed Handshake is illustrated in Figure 6.

In the high speed mode, the Answer modem sends a 2400 Hz scrambled mark out slightly after detection of the Originate modem's 1200 Hz mark. Both Originate and Answer modems send data on the termination of their respective transmitted marks. The high speed handshake is illustrated in Figure 7.

3

ORIGINATING STATION

RECEIVE CARRIER — ANSWER TONE —

DATA

1270 Hz

TRANSMIT CARRIER

DATA

FSK CD

0.15 S

PSK CD

ANSWERING STATION

RECEIVE CARRIER

DATA

TRANSMIT CARRIER

DATA

FSK CD

PSK CD

— 0.890 S —

— 0.33 S —

0.15 S
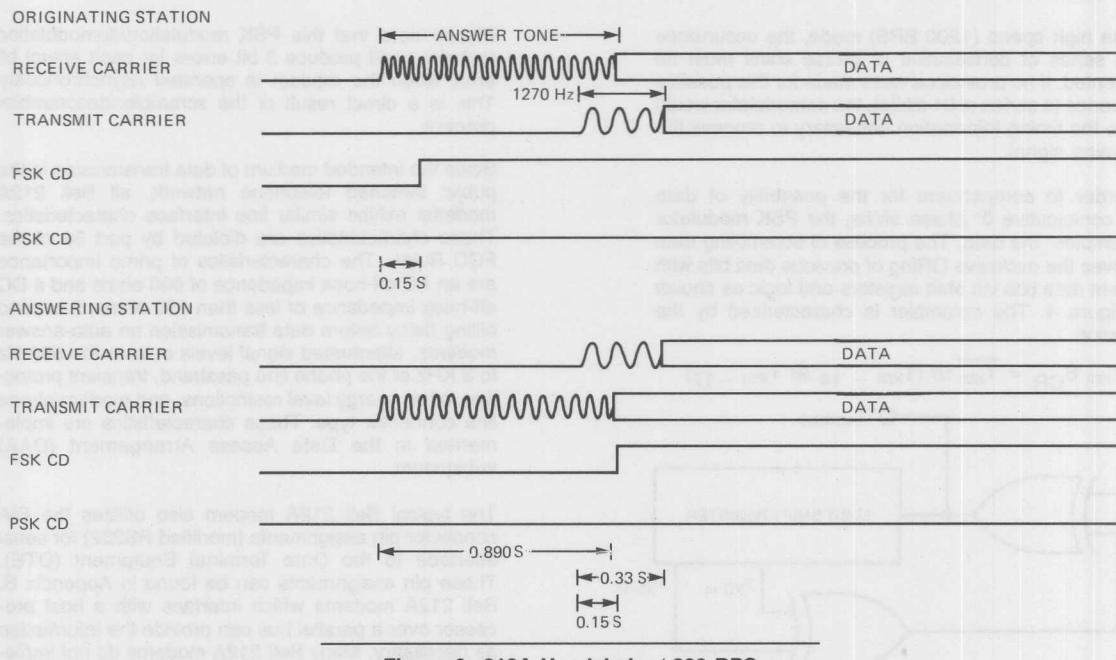
Figure 6. 212A Handshake / 300 BPS

ORIGINATING STATION

RECEIVE CARRIER — ANSWER TONE — 2400 Hz MARK *

— 1200 Hz MARK —

DATA

TRANSMIT CARRIER

DATA

FSK CD

PSK CD

0.15 S   0.27 S

ANSWERING STATION

RECEIVE CARRIER — 1200 Hz MARK —

DATA

BILLING DELAY — ANSWER TONE — 2400 Hz MARK *

TRANSMIT CARRIER

DATA

FSK CD

PSK CD

2 S — 1 S — 0.774 S —

— 1.32 S —

0.27 S
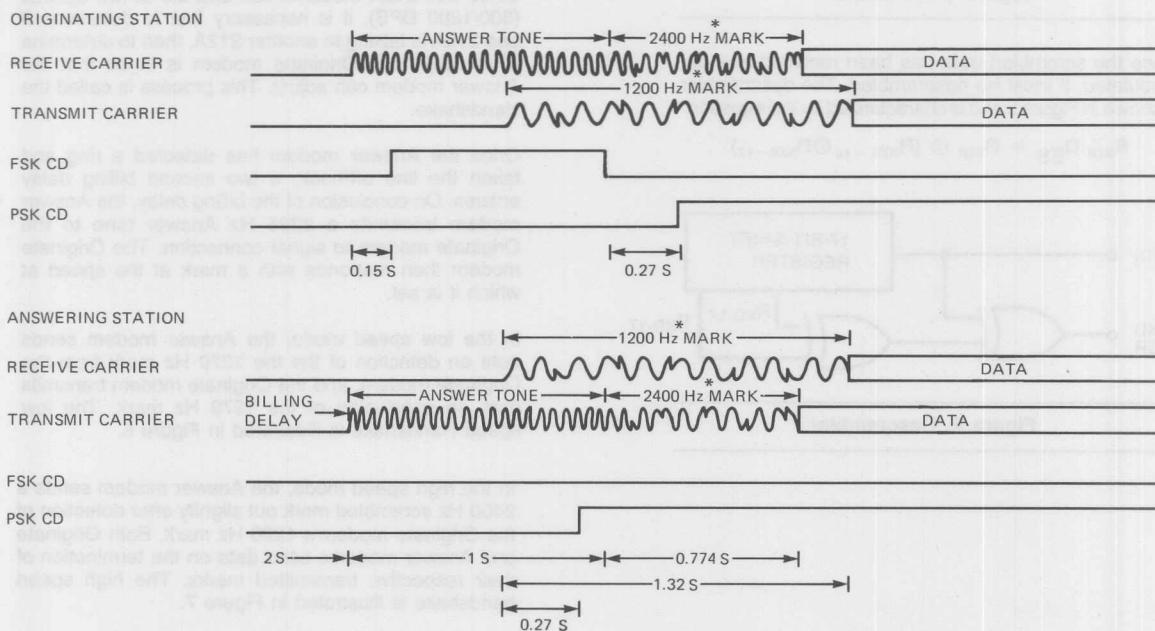
Figure 7. 212A Handshake / 1200 BPS

*Denotes SCRAMBLED

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FEATURES

Bell 212A features often include auto-answer, analog and digital loop testing, and dialer functions.

The auto-answer feature requires a method of detecting the 20 Hz ring signal. Since the ring signal varies from 45 to 150 V_{rms} and there is the possibility of a high voltage line transient, the ring indicator must be isolated from the modem which typically runs off a much lower potential. This is executed with an opto-isolator as shown in Figure 8.
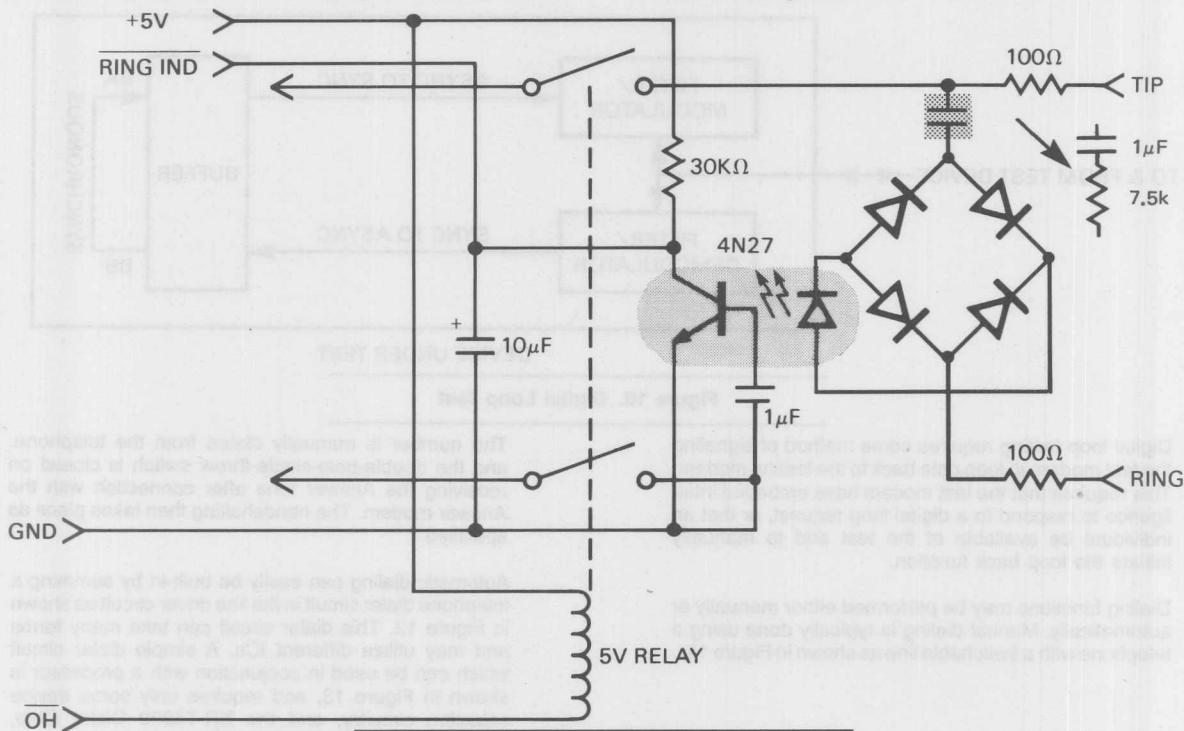
Figure 8. Ring Detect

The 5 V relay is used to put the modem "off-hook" and on-line on a ring detect. This is performed before the secondary of the line isolation transformer. Once the modem has been taken off-hook, the previously described Handshake sequence beings.

Analog loop testing takes a number of forms, but the basic premise is the same: loop the modulated carrier from the TXC filter output into the demodulator receive input, bypassing the receive filter (see Figure 9). The three variations of this basic concept are analog loop test, self-test analog loop, and end-to-end self-test. These variations are illustrated in Appendix C.

(SHOWN IN LOOPBACK CONDITION)
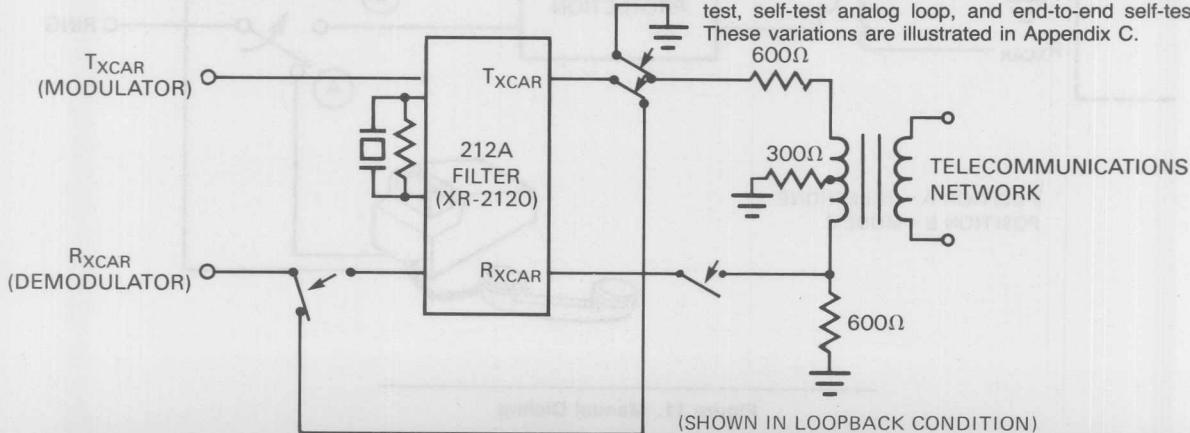
Figure 9. Analog Loopback

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Digital loop testing exercises the full capabilities of the Bell 212A modem. The digital loop test forces demodulation, modulation and filtering by the modem under test. Figure 10 illustrates the basic digital loop test, and Appendix D contains diagrams depicting remote digital loop, self-test remote digital loop, digital loop, and self-test digital loop.
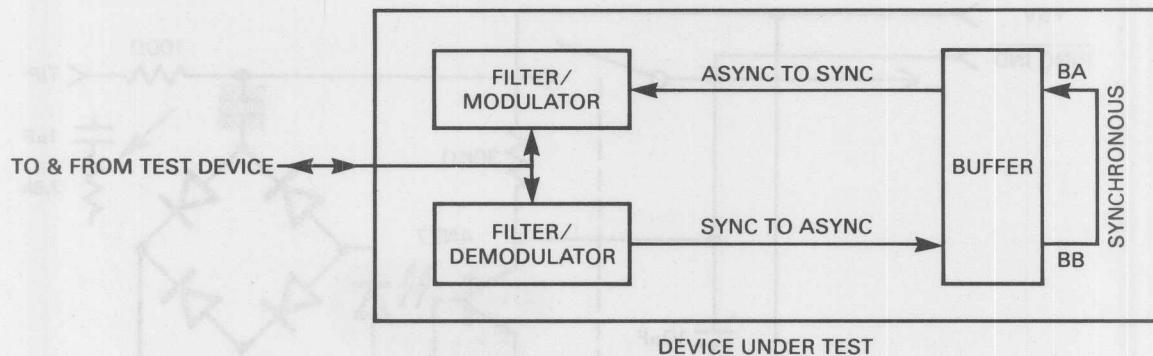

Figure 10. Digital Loop Test

Digital loop testing requires some method of signaling the test modem to loop data back to the testing modem. This requires that the test modem have embeded intelligence to respond to a digital loop request, or that an individual be available at the test end to manually initiate the loop back function.

Dialing functions may be performed either manually or automatically. Manual dialing is typically done using a telephone with a switchable line as shown in Figure 11.

The number is manually dialed from the telephone, and the double-pole-single-throw switch is closed on receiving the Answer tone after connection with the Answer modem. The handshaking then takes place as specified.

Automatic dialing can easily be built-in by summing a telephone dialer circuit in the line driver circuit as shown in Figure 12. This dialer circuit can take many forms and may utilize different ICs. A simple dialer circuit which can be used in conjunction with a processor is shown in Figure 13, and requires only some device selection circuitry, and the XR-T5990 Dialer Chip, whose output is summed into the line driver.

POSITION A = TELEPHONE
POSITION B = MODEM
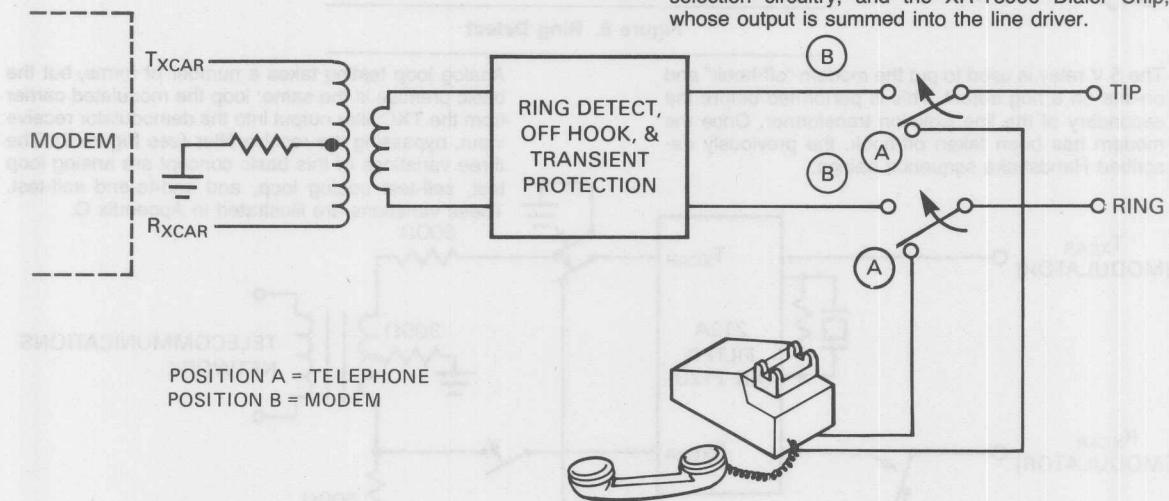
**Figure 11. Manual Dialing**
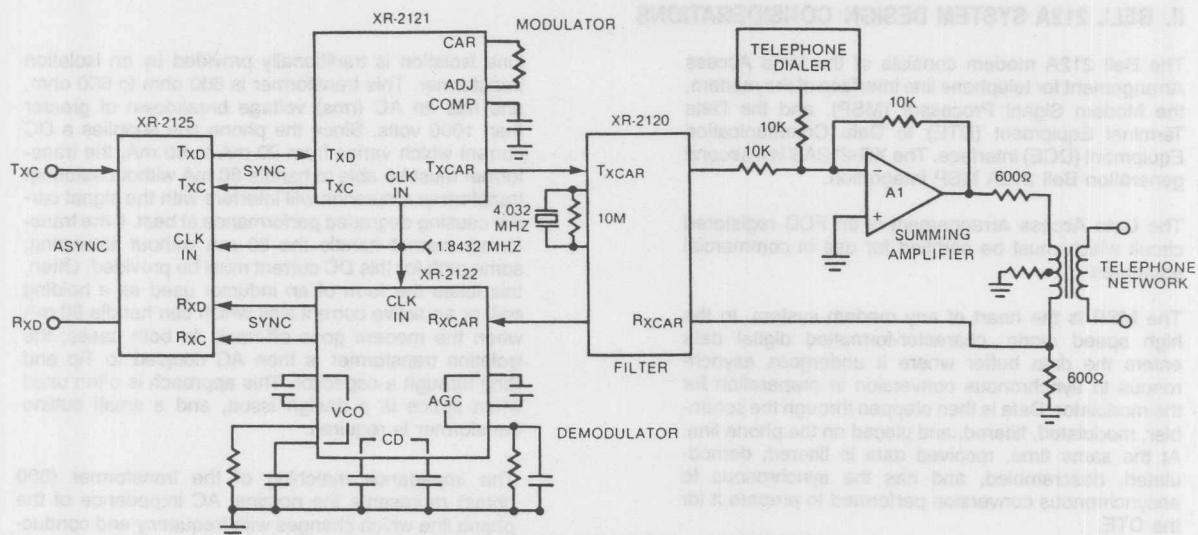
**Figure 12. Implementing the Telephone Dialing Function**
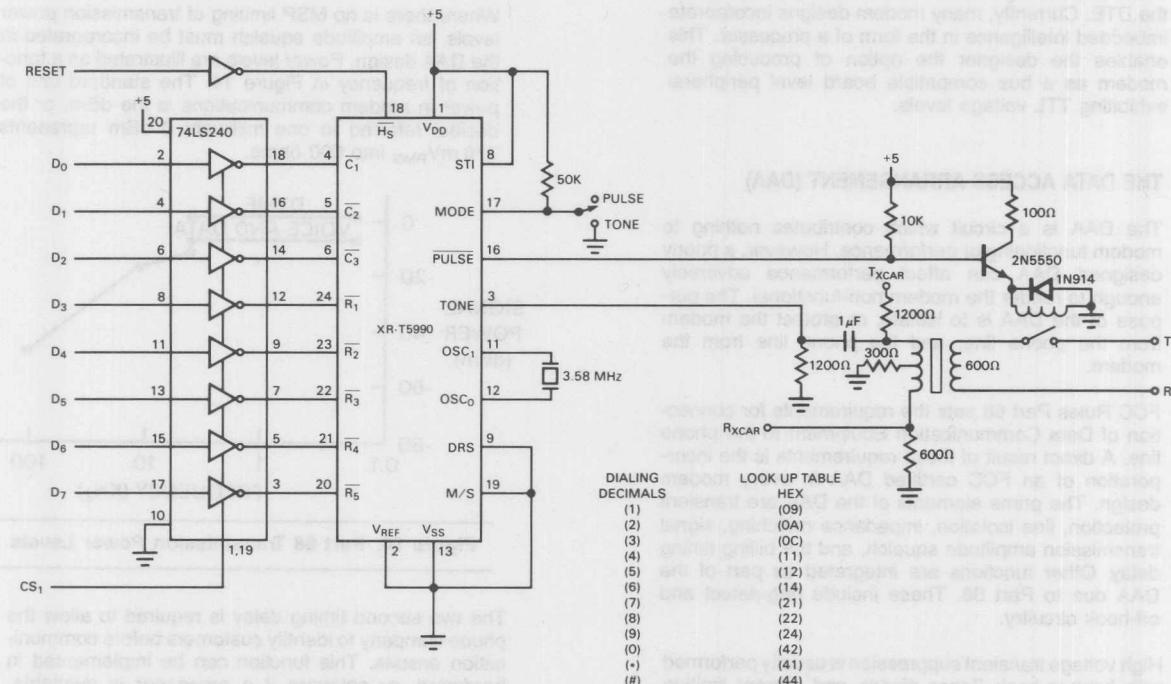
Figure 13. A Processor Controlled Dialer

The dialer of Figure 13 will require a look-up table to generate row/column data from user numerical input, which will typically come from a terminal or host processor.

II. BELL 212A SYSTEM DESIGN CONSIDERATIONS

The Bell 212A modem consists of the Data Access Arrangement for telephone line interface of the modem, the Modem Signal Processor (MSP), and the Data Terminal Equipment (DTE) to Data Communication Equipment (DCE) interface. The XR-212AS is a second generation Bell 212A MSP integration.

The Data Access Arrangement is an FCC registered circuit which must be certified for use in commercial equipment.

The MSP is the heart of any modem system. In the high speed mode, character-formatted digital data enters the data buffer where it undergoes asynchronous to synchronous conversion in preparation for the modulator. Data is then stepped through the scrambler, modulated, filtered, and placed on the phone line. At the same time, received data is filtered, demodulated, descrambled, and has the synchronous to ansynchronous conversion performed to prepare it for the DTE.

The front-end of the modem is the DCE/DTE interface. Previously, this consisted of translating demodulated and modulated data voltage levels to and from RS-232C data voltage levels for serial communication to the DTE. Currently, many modem designs incorporate imbedded intelligence in the form of a processor. This enables the designer the option of producing the modem as a bus compatible board level peripheral exhibiting TTL voltage levels.

THE DATA ACCESS ARRANGEMENT (DAA)

The DAA is a circuit which contributes nothing to modem functioning or performance. However, a poorly designed DAA can affect performance adversely enough to render the modem non-functional. The purpose of the DAA is to isolate, or protect the modem from the phone line, and the phone line from the modem.

FCC Rules Part 68 sets the requirements for connection of Data Communication Equipment to the phone line. A direct result of these requirements is the incorporation of an FCC certified DAA in every modem design. The prime elements of the DAA are transient protection, line isolation, impedance matching, signal transmission amplitude squelch, and the billing timing delay. Other functions are integrated as part of the DAA due to Part 68. These include ring-detect and off-hook circuitry.

High voltage transient suppression is usually performed with back-to-back Zener diodes and current limiting resistors. Transient protection should provide a path to ground for voltages of greater than 1500 V_{peak}. Zener protection may also be provided on the secondary side to protect modem equipment.

Line isolation is traditionally provided by an isolation transformer. This transformer is 600 ohm to 600 ohm, and has an AC (rms) voltage breakdown of greater than 1000 volts. Since the phone line supplies a DC current which varies from 20 mA to 80 mA, the transformer must be able to handle 80 mA without saturing: transformer saturation will interfere with the signal carrier causing degraded performance at best. If the transformer cannot handle the 80 mA without saturating, some path for this DC current must be provided. Often, this takes the form of an inductor used as a holding coil, or an active current sink which can handle 80 mA when the modem goes off-hook. In both cases, the isolation transformer is then AC coupled to Tip and Ring through a capacitor. This approach is often used when space is a design issue, and a small outline transformer is required.

The impedance matching of the transformer (600 ohms) represents the nominal AC impedance of the phone line which changes with frequency and conductor type and size (see Appendix A). The DC resistance presented to the line by the transformer should be less than 200 ohms to adequately hold the line off-hook for the phone company.

Where there is no MSP limiting of transmission power levels, an amplitude squelch must be incorporated in the DAA design. Power levels are illustrated as a function of frequency in Figure 14. The standard unit of power in modem communications is the dBm, or the decibel referred to one milliwatt; 0 dBm represents 776 mV_{RMS} into 600 ohms.
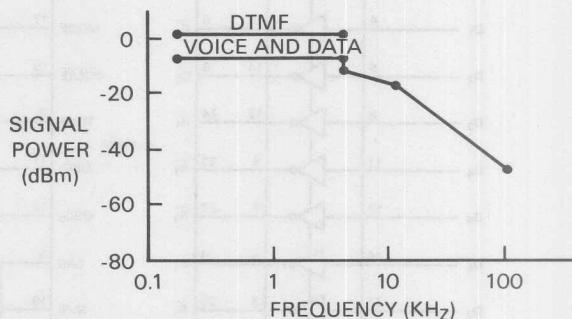
Figure 14. Part 68 Transmission Power Levels

The two second timing delay is required to allow the phone company to identify customers before communication ensues. This function can be implemented in hardware, or software if a processor is available. A simple hardware implementation of the delay is an XR-555 timer which is triggered by the modem off-hook and which delays the RTS signal on the RS-232C. If a processor is available as the modem controller, it is probably more efficient and convenient to implement a software counter.

The ring-detect circuit senses the ring signal which may vary from 40 V_{rms} to 150 V_{rms} and which rides on the DC line voltage of 42.5 V to 62.5 V at a nominal 20 Hz. The ring-detect circuit is capacitively coupled to Tip and Ring and must present an AC impedance of 1.6 K ohms to 40 K ohms to the phone line. The smaller the impedance presented to the line, the larger the ringer equivalence number (REN) – a figure directly proportional to the number of telecommunication devices which may be attached to the line. The circuit is typically designed around an opto-isolator with a minimum breakdown voltage of 1000 V_{rms}.

Once the ring signal has been detected, the modem must be placed off-hook. This is easily performed using a relay such as a Clare LBP0060B00. The relay must also exhibit a minimum breakdown voltage of 1000 V_{rms}.

Transmit/receive carrier separation is accomplished by using a hybrid transformer with a center-tapped secondary (device-line side) as in Figure 15, or by implementing a hybrid circuit as in Figure 16. The disadvantage of the hybrid circuit is that its effectiveness depends on the phone line impedance, which varies as implied by Appendix A.
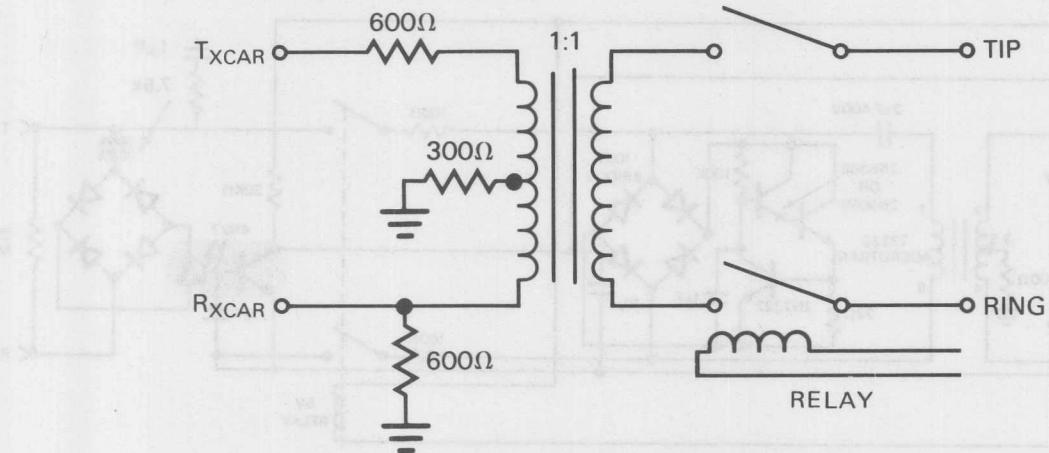

Figure 15. Hybrid Transformer Transmit/Receive Isolation

*OPTIONAL, ONLY USED TO BUFFER T_{XCAR} PATH
OP AMPS = XR-4558
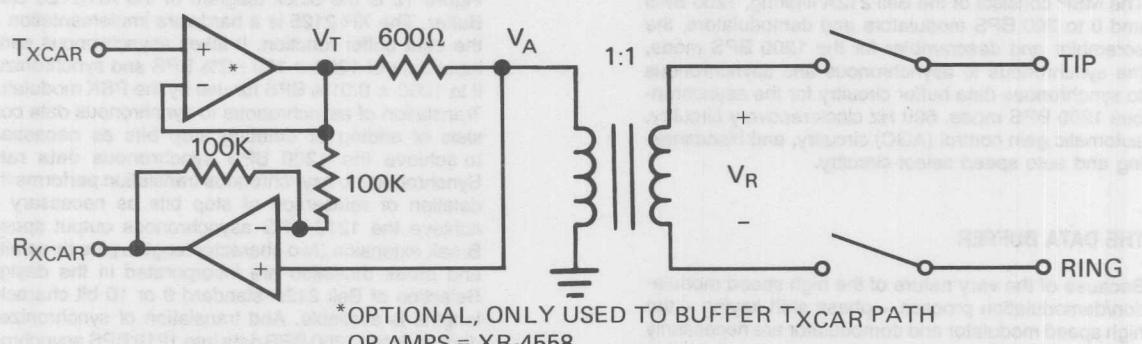
Figure 16. Hybrid Circuit Transmit/Receive Isolation

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Hybrid circuit signal separation is accomplished in the following fashion. The transmit signal, T_{XCAR}, is halved at the output by the voltage divider presented by the transformer impedance (nominally 600 ohms) and the 600 ohm resistor on the output of the transmit amplifier. The receive signal, R_{XCAR}, is doubled by the receive amplifier which also multiplies the transmit amplifier output, V_T, by a negative one, and the secondary voltage due to the transmit carrier, $V_T/2$, by two, cancelling out V_T and providing a receive amplifier output of 2 V_R. Again, note that as line impedances vary, so will the ability of the hybrid circuit to separate transmit/receive signals.

Figure 17 is an example of DAA hardware design. Impedance matching and transmit/receive carrier separation is the function of the center-tapped, 600 ohm terminated Microtran T2220 transformer. The back-to-back Zener diodes with the series 100 ohms provide the transient protection. The primary side of the transformer is capacitively coupled and uses a rectifier, a darlington pair, and a 2N2222 transistor to actively sink the DC holding current. The final stage consists of the opto-isolator circuit (4N27), and a 5 V relay. It is assumed that billing delay timing is implemented elsewhere (in the MSP) in hardware or software and the transmit power squelch circuitry is unnecessary if power levels have been permanently and restrictively (no customer gain options) set.
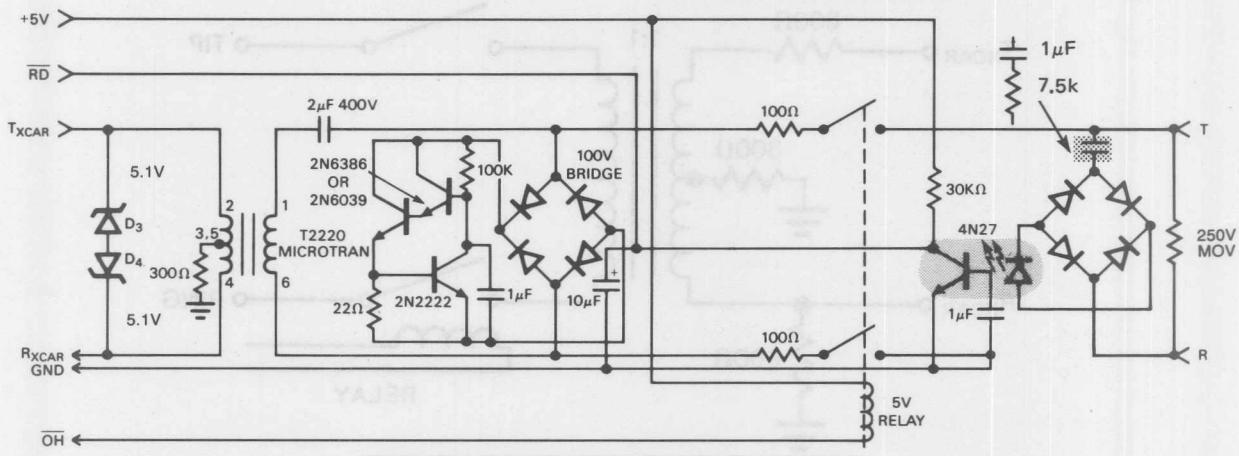
Figure 17. The DAA Circuit

THE MSP

The MSP consists of the Bell 212A filtering, 1200 BPS and 0 to 300 BPS modulators and demodulators, the scrambler and descrambler for the 1200 BPS mode, the synchronous to asynchronous and asynchronous to synchronous data buffer circuitry for the asynchronous 1200 BPS mode, 600 Hz clock recovery circuitry, automatic gain control (AGC) circuitry, and Handshaking and auto speed select circuitry.

THE DATA BUFFER

Because of the very nature of the high speed modulation/demodulation process – phase shift keying – the high speed modulator and demodulator are necessarily synchronous. The low speed frequency shift keying modulation/demodulation process – generating distinct frequencies to represent data and sensing those frequencies – allows for a completely bit-asynchronous modulation/demodulation process.

Figure 18 is the block diagram of the XR-2125 Data Buffer. The XR-2125 is a hardware implementation of the data buffer function. It takes asynchronous serial input data of 1200 +1%/−2% BPS and synchronizes it to 1200 ± 0.01% BPS for use by the PSK modulator. Translation of asynchronous to synchronous data consists of adding or deleting stop bits as necessary to achieve the 1200 BPS synchronous data rate. Synchronous to asynchronous translation performs the deletion or reinsertion of stop bits as necessary to achieve the 1219 BPS asynchronous output speed. Break extension (two character lengths plus three bits) and break detection are incorporated in the design. Selection of Bell 212A standard 9 or 10 bit character lengths is available. And translation of synchronized, demodulated 1200 BPS data into 1219 BPS asynchronous data is performed. The XR-2125 also provides transmit and receive enable ($T_{X\,EN}$ and $R_{X\,EN}$) selection so that the data buffer may be disabled for 300 BPS (0 to 300 BPS) or synchronous 1200 BPS.

Implementation of this function in software in a processor-based design is fairly straight forward. A software data buffer which handles the 8 to 11 bit V.22 CCITT character lengths is also easily implemented, and available from Exar's application department.
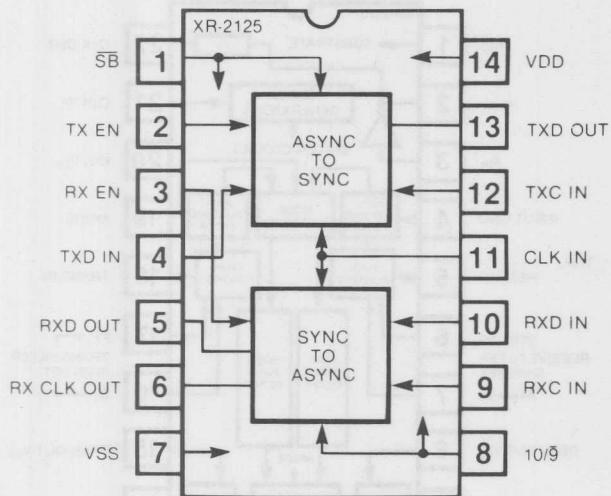
Figure 18. XR-2125 Data Buffer

Figure 19. XR-2121 Modulator

THE 212A MODULATOR

The Bell 212A modulator consists of the high speed 1200 BPS PSK modulator circuitry, and the low speed 0 to 300 BPS FSK modulator. The PSK modulator encodes two bits simultaneously into a dibit which is represented by a phase shift (see Figure 2) of the carrier frequency (1200 Hz for the Originate modem's transmit mode and 2400 Hz for the Answer modem's transmit mode). This modulation process requires a scrambler to pre-scramble data because of the potential of generating a string of 0° phase shifts. Such a string of modulated data would confuse the Answer modem's clock recovery circuitry, causing the inaccurate demodulation of data. The FSK modulator generates two separate frequencies to represent digital ones (marks) and zeros (spaces). In the Originate mode, transmit marks are 1270 Hz and spaces are 1070 Hz. In the Answer mode, transmit marks are 2225 Hz and spaces are 2025 Hz.

PSK data communication occurs at 600 baud because of its dibit encoding modulation technique. FSK data communication occurs at a rate of one bit per baud up to a rate of 300 baud.

Figure 19 is a functional block diagram of the XR-2121. The integrated scrambler is the same as that shown in Figure 4. The PSK modulator utilizes digital echo modulation techniques for carrier generation. This allows the shaping, or band limiting, of the transmitted modulated carrier and produces adjacent channel crossover frequency rejection of approximately 40 dB. This high degree of rejection reduces the probability of wrap around of the transmit harmonics into the received carrier. The coefficients for producing the transmitted carrier spectrum are stored in a mask-alterable PROM and produce a raised-cosine type roll-off. The 1200/300 and MODE pins toggle from high speed to low speed, and from Answer to Originate modes. The scrambler enable pin ($S_{CR\ EN}$) is kept high for both 300 BPS and 1200 BPS. It is normally used for V.22 handshaking.
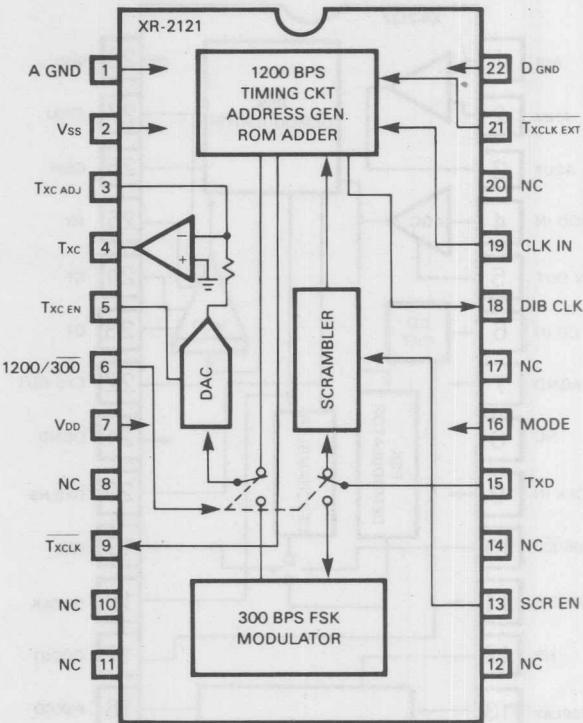
FSK carrier generation is performed using a sine look-up table. The output synthesized sine wave consists of 12 steps. Frequency transitions are phase coherent to maintain a low bias distortion in the demodulated receive carrier.

THE 212A DEMODULATOR

The demodulation related circuitry (Figure 20) is integrated into the XR-2122 Bell 212A Type Demodulator. Included is the 212A 1200 BPS demodulation circuitry as well as the descrambler, the 600 Hz baud clock recovery circuitry, the automatic gain control (AGC) amplifier, the carrier detect circuitry for energy, PSK, and FSK (this circuitry facilitates the handshaking protocol and auto speed select).

The 0 to 300 BPS FSK demodulation process is phase-locked loop based and offers low bias and jitter distortion.

The 1200 BPS PSK demodulation process provides coherent demodulation characteristic of its Costas Loop for carrier recovery. The Costas Loop approach to demodulation allows the flexibility to meet a ±7 Hz frequency translation specification as well as providing access to an eye diagram for use in adjusting for optimum BER vs. S/N performance (12 dB typical for 10^{-5} BER for worst case line conditions).

11
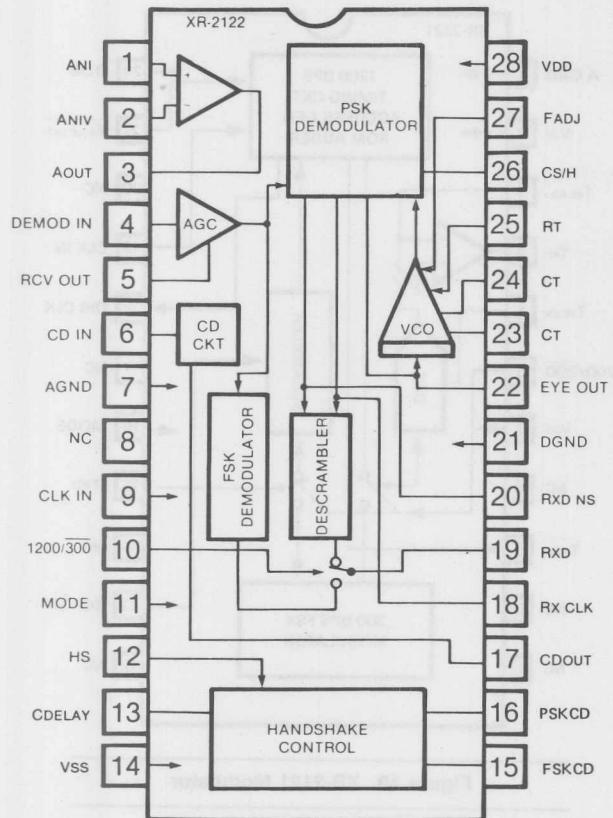
Figure 20. XR-2122 Demodulator

Figure 21. The XR-2120 212A Modem Switched Capacitor Filter

The integrated descrambler is the same as that shown in Figure 5. Integration of the clock recovery circuitry, AGC amplifier, and carrier detect circuitry completes the MSP circuitry with the exception of the handshaking protocol and auto speed select logic. Exclusion of this logic from the XR-2122 allows protocol flexibility for processor-based designs: the handshaking and auto-speed select cost very little in software/hardware design overhead.

THE 212A MODEM FILTER

The XR-2120 212A Modem Switched Capacitor Filter (Figure 21) offers a pair of 24th order bandpass filters; one for the transmit path and one for the receive path. Each path has a two pole low pass anti-aliasing filter to eliminate spurious switching frequency harmonics from affecting the performance of the 20th order, equalization and bandpass filters. Center frequencies for the two filters are 1200 Hz and 2400 Hz. Two poles of output active filtering for wave shaping are provided in each signal path. The transmit and receive gain may be digitally controlled to increase overall gain by as much as 14 dB. And center frequencies may be shifted down by integral division of the crystal generated clock frequency.

The XR-2129 filter will generate the 1.8432 MHz clock for the XR-2121 Modulator, XR-2122 Demodulator, and the XR-2125 Data Buffer. The XR-2129 also provides analog loopback capability and worst case line equalization.

III. THE XR-212AS MSP APPLICATION CIRCUIT

Figure 22 shows the essential Bell 212A MSP as realized with the XR-212AS chip set. In order to meet Bell specifications, the MSP also requires additional logic and timing circuitry to utilize the FSK and PSK carrier detect circuitry for Handshaking purposes and auto speed select. To achieve both synchronous and asynchronous communication, some provision must also be made to toggle the T_{XEN} and R_{XEN} pins of the XR-2125 as well as the SCR EN pin of the XR-2121 and the RXDNS pin of the XR-2122.

Given the additional circuitry for the Handshaking, and the manual speed select, Figure 22 represents a complete MSP for a dumb 212A modem. See the parts list in AN-28, page 57.

Also, the Handshake, and auto and manual speed select can be easily performed with a microprocessor, which most applications incorporate into the design.

Figure 22. The XR-212AS MSP

13
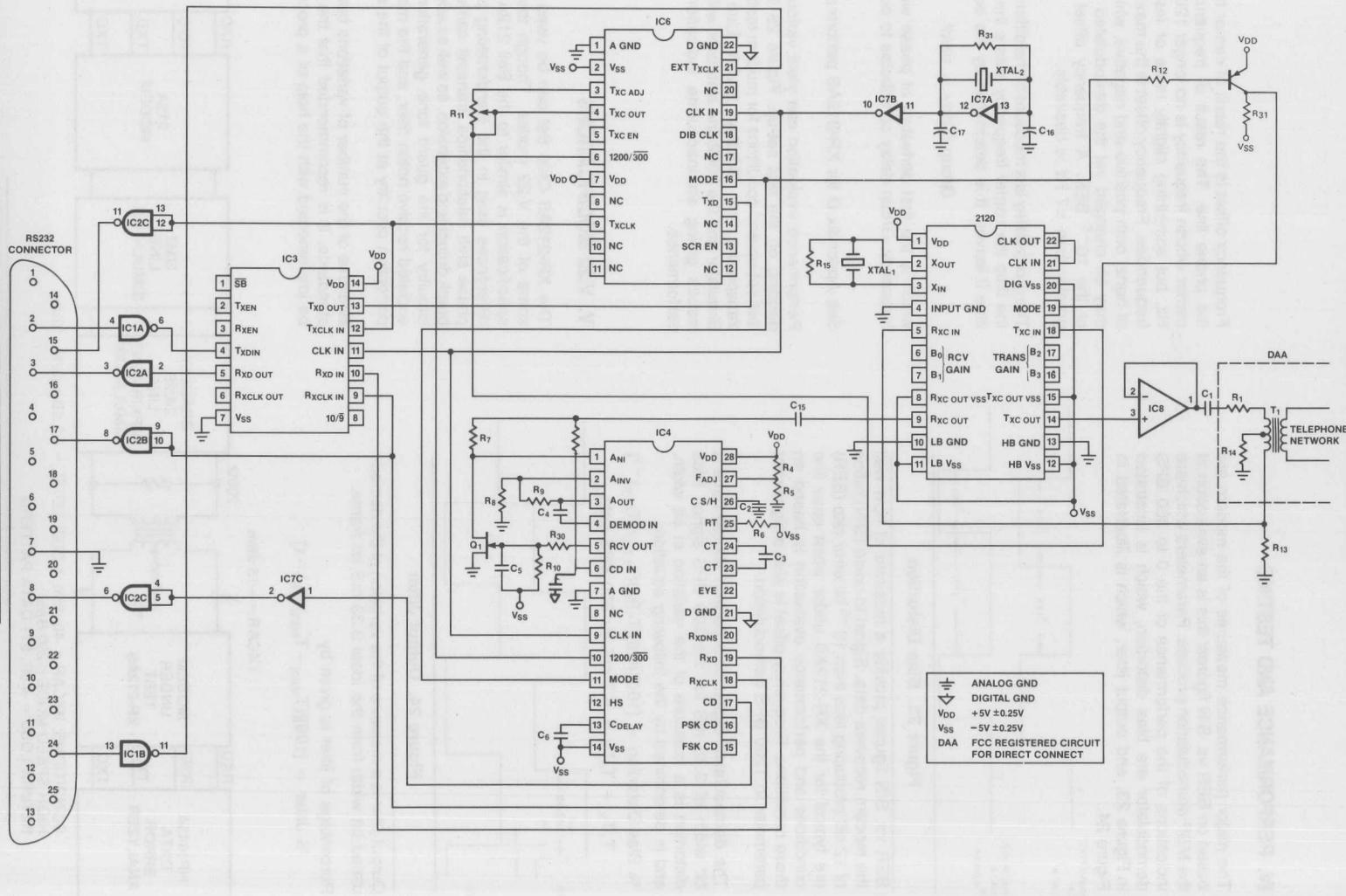
IV. PERFORMANCE AND TESTING

The major performance measures of the modem are based on BER vs. S/N figures: this is an evaluation of the MSP demodulation process. Parameters which are indications of the performance of the 0 to 300 BPS demodulator are bias distortion, which is illustrated in Figure 23, and output jitter, which is illustrated in Figure 24.
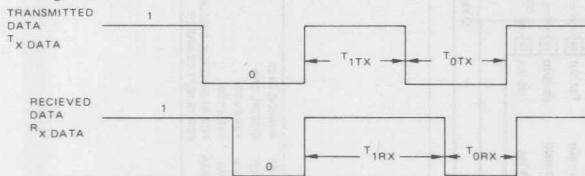

Figure 23. Bias Distortion

BER vs. S/N figures provide a measure of how well the modem recovers data. Signal to noise (S/N) ratios of 12 dB producing less than 10^{-5} bit error rate (BER) are typical for the XR-212AS under worst case line conditions and performance evaluation is based on those conditions. Frequency offset is also a significant parameter in 1200 BPS demodulation.

The demodulated digital data pattern should have a bit width of 3.33 mS for the 300 BPS signal. Bias distortion is a measure of the variation in bit width, and is determined by the following equation:

$$\% \text{ Bias Distortion} = [100][(0.5)(T_1 R_X)(T_{1TX} + T_{0TX})^{-1}]$$

$$T_1 T_X + T_0 T_X = 6.7 \text{ mS for 300 BPS data.}$$
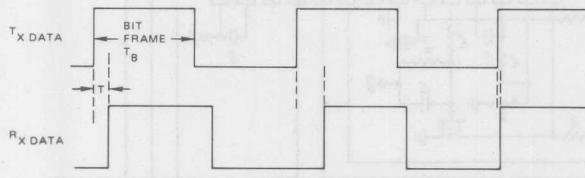
Figure 24. Output Jitter

Output jitter is a measure of the variation of the demodulated bit width from the ideal 3.33 mS bit frame.

Percentage of jitter is given by

$$\% \text{ Jitter} = [100][(T_{MAX} - T_{MIN})(T_B) - 1]$$

Frequency offset is the result of carrier heterodyne by the phone line. The result of frequency offset is a carrier whose frequency is no longer 1200 Hz or 2400 Hz, but something slightly more or less then those frequencies. Frequency offset is the maximum number of hertz, both positive and negative, which the carrier may be changed yet the demodulated data remains at the 10^{-5} BER. A frequency offset tolerance of greater than ± 7 Hz is desirable.

The group delay is a measure of the difference between the time the carrier frequency enters the filter and the time it leaves. It is determined by the equation

$$\text{Group Delay} = d\theta/df$$

which is the first derivative of phase with respect to frequency. Group delay contributes to output jitter.

See Appendix D for XR-212AS performance figures.

Performance evaluation can yield various results depending on the test set-up. Figure 25 illustrates the test set-up and conditions for modem testing. Note that transposing the Bradley 2A/2B Line Impairment Simulator and the 3002 line simulator will improve test results giving an inaccurate indication of modem performance.

V. V.22 MODIFICATIONS

The XR-212AS Chip Set can be used to implement some of the V.22 modes. Though the CCITT V.22 specification is similar to the Bell 212A specification, differences exist in the Handshaking protocol, data/ phase shift relationships, transmit carrier length, and break detect and extension, as well as additional CCITT circuitry for the guard tone generation and its associated receive notch filter, and the mark detect and correction circuitry at the output of the scrambler.

Because of the number of variations between the two standards, it is recommended that the V.22 modem be implemented with the help of a processor.

CONDITIONS: RXCAR = -40 dbm, NOISE LEVEL = -52 dBm (S/N = 12db), HIGH SPEED MODE (1200 Bps)
RETURN LOSS = -4 dB, 511 DATA PATTERN

**Figure 25. Test Set-Up and Conditions**

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HANDSHAKE PROTOCOL

The V.22 Handshake sequence for alternatives A and B is shown in Figure 26. With the exception of the 2100 Hz Answer Tone, and the use of the unscrambled binary one as part of the Handshake, the timing, scrambling, and frequency of the rest of the Handshake are similar to those of the Bell 212A.

Generation of the 2100 Hz Answer Tone can be accomplished using the XR-2206. Figure 27 illustrates a circuit which realizes this function.

The V.22 handshake requires the sending of an unscrambled binary one for 511 ± 60 ms. The XR-2122 does not recognize this as a part of the handshake protocol. However, detection of this condition and subsequent activation of the XR-2122 handshake circuitry is easily accomplished in software. Generation of the unscrambled binary one is achieved by disabling the XR-2121 scrambler and transmitting a mark or binary one.
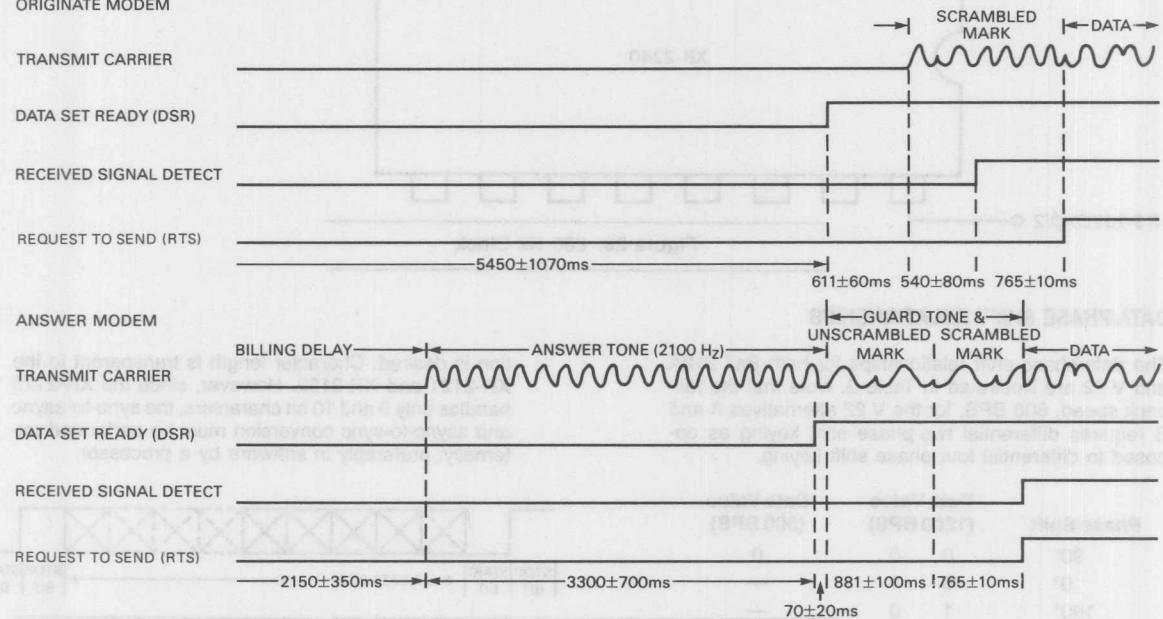
Figure 26. V.22 Handshake
(With V.25 Auto Answer)

f = 2100Hz
R_1 = 475 Ω 1%
C = 0.01µF
V+= +5V
V- = -5V
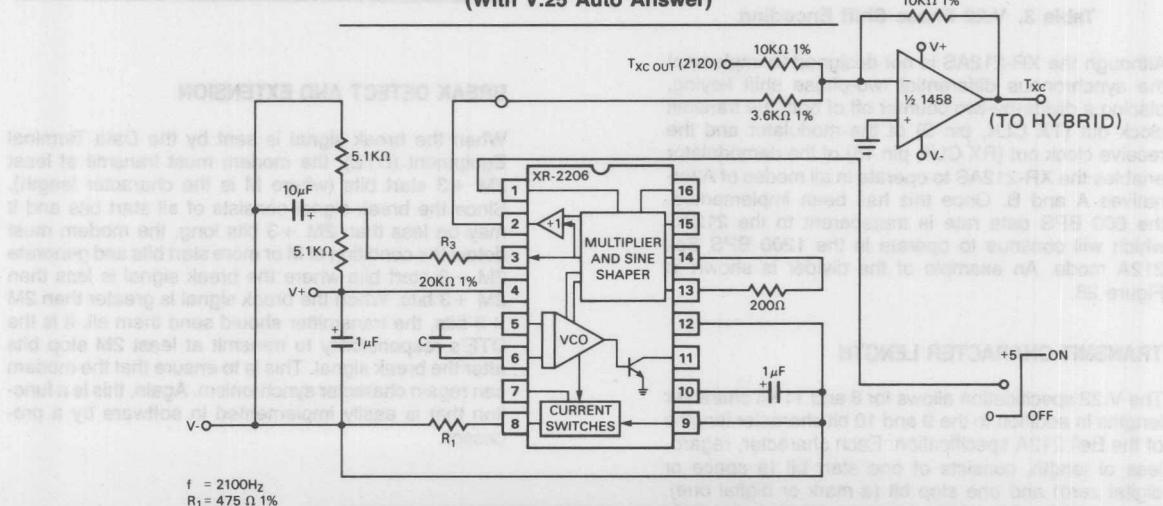
Figure 27. Answer Tone Generation
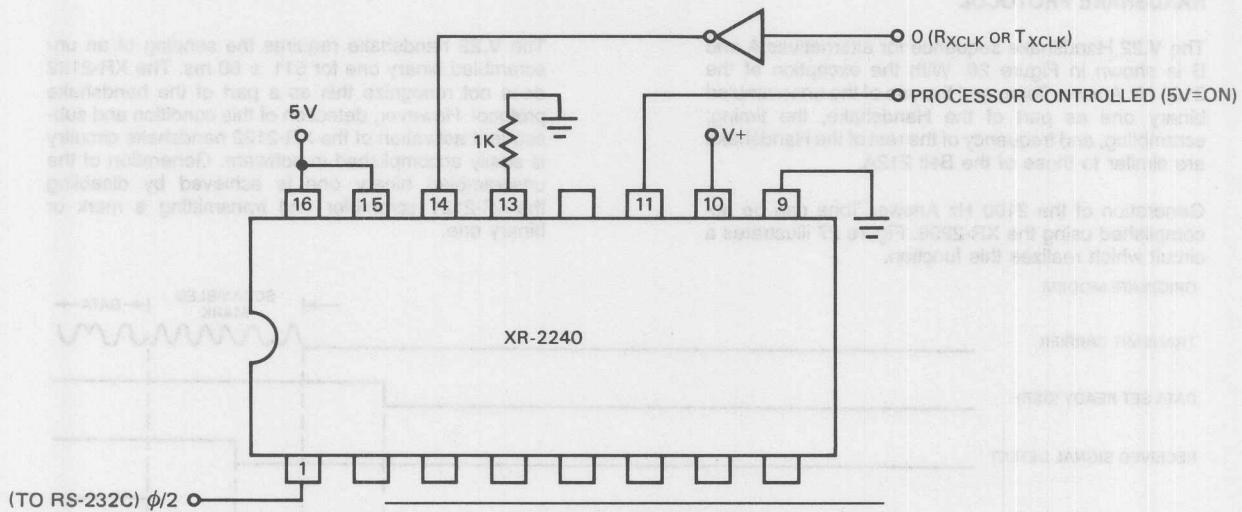
Figure 28. 600 Hz Clock

DATA/PHASE SHIFT RELATIONSHIPS

The data/phase shift relationships for both Bell 212A and V.22 are illustrated in Table 3. Note that the fallback speed, 600 BPS, for the V.22 alternatives A and B requires differential two-phase shift keying as opposed to differential four-phase shift keying.

Phase Shift	Data Value (1200 BPS)		Data Value (600 BPS)
90°	0	0	0
0°	0	1	—
100°	1	0	—
− 90°	1	1	1

Table 3. V.22 Phase Shift Encoding

Although the XR-212AS is not designed to implement the synchronous differential two-phase shift keying, placing a divide-by-two counter off of both the transmit clock out (TX CLK, pin 9) of the modulator and the receive clock out (RX CLK, pin 18) of the demodulator enables the XR-212AS to operate in all modes of Alternatives A and B. Once this has been implemented, the 600 BPS data rate is transparent to the 212AS which will continue to operate in the 1200 BPS Bell 212A mode. An example of the divider is shown in Figure 28.

TRANSMIT CHARACTER LENGTH

The V.22 specification allows for 8 and 11 bit character lengths in addition to the 9 and 10 bit character lengths of the Bell 212A specification. Each character, regardless of length, consists of one start bit (a space or digital zero) and one stop bit (a mark or digital one). The remaining bits of the character represent a data word. Provision is made to allow replacement of data bits by additional stop bits if such a character varia-tion is desired. Character length is transparent to the XR-2121 and XR-2122. However, since the XR-2125 handles only 9 and 10 bit characters, the sync-to-async and async-to-sync conversion must be performed externally; preferably in software by a processor.
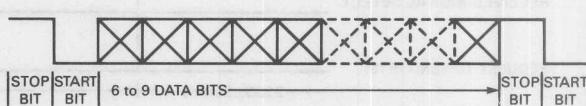
Figure 29. Transmit Character Length

BREAK DETECT AND EXTENSION

When the break signal is sent by the Data Terminal Equipment (DTE), the modem must transmit at least 2M +3 start bits (where M is the character length). Since the break signal consists of all start bits and it may be less than 2M +3 bits long, the modem must detect the condition of M or more start bits and generate 2M +3 start bits where the break signal is less than 2M +3 bits. When the break signal is greater than 2M +3 bits, the transmitter should send them all. It is the DTE's responsibility to transmit at least 2M stop bits after the break signal. This is to ensure that the modem can regain character synchronism. Again, this is a function that is easily implemented in software by a processor.

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GUARD TONE GENERATION AND FILTERING

V.22 specifications require that the answer modem send either an 1800 Hz or 550 Hz guard tone with the transmitted data when operating in the high speed mode. The amplitude of the guard tone should be 6 ± 1 dB lower than that of the data power level. Figure 30 is a guard tone generation ciruit.

The data carrier frequency must be extracted from the guard tone when received at the originate modem. This is accomplished by placing notch filters in front of the XR-2120. Figure 31 A and B are the 550 Hz and 1800 Hz notch filters.
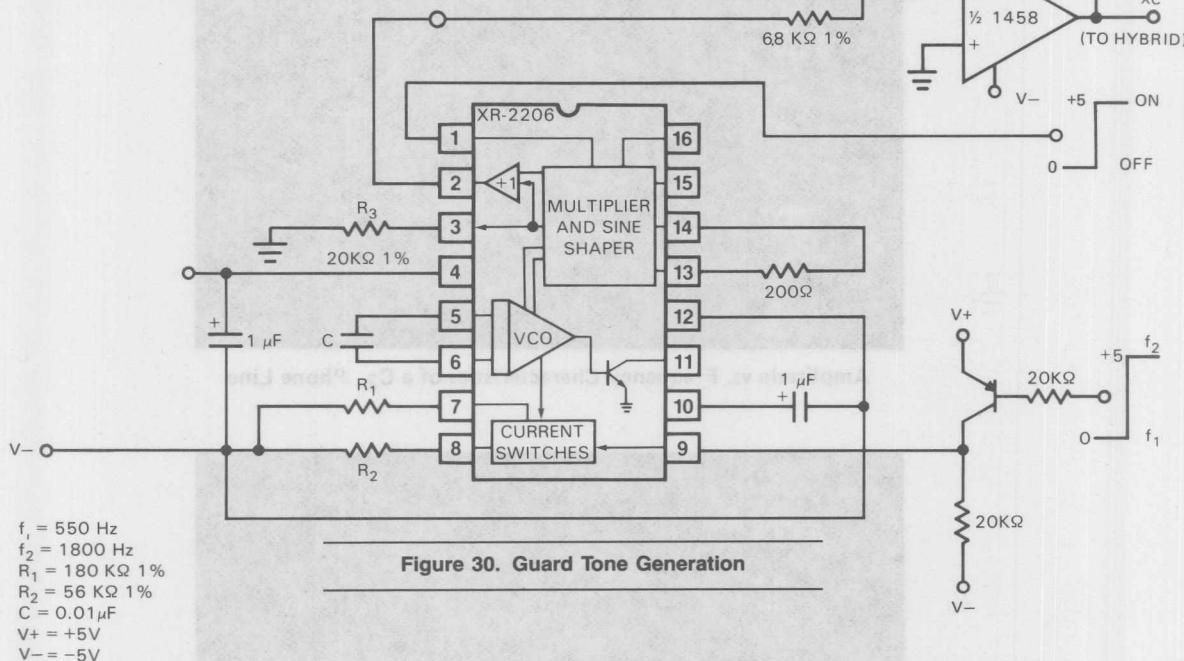
MARK DETECT AND CORRECTION

V.22 specifies the inclusion of circuitry which will detect a sequence of 64 consecutive binary ones and, on detection, will invert the next output from the scrambler. This function is implemented in the XR-212.

$f_1 = 550$ Hz
$f_2 = 1800$ Hz
$R_1 = 180$ KΩ 1%
$R_2 = 56$ KΩ 1%
$C = 0.01\mu$F
$V+ = +5$V
$V- = -5$V

Figure 30. Guard Tone Generation
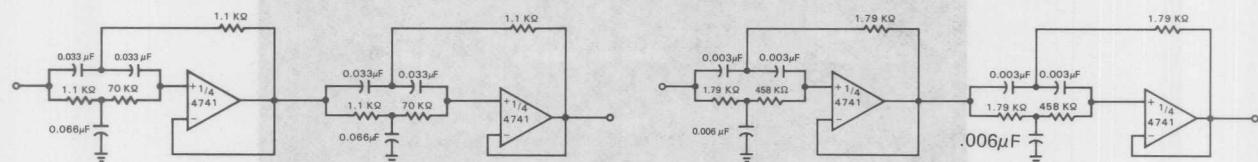
Figure 31A and 31B. V.22 Notch Filters

17

APPENDIX A
## Telephone Line Characteristics
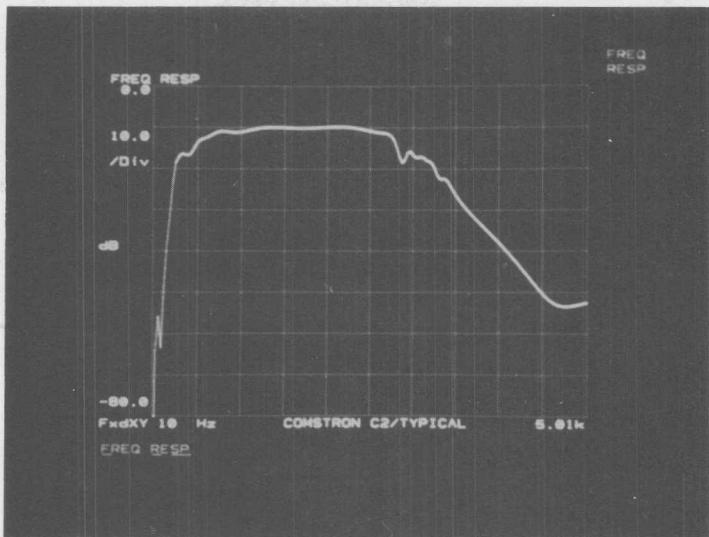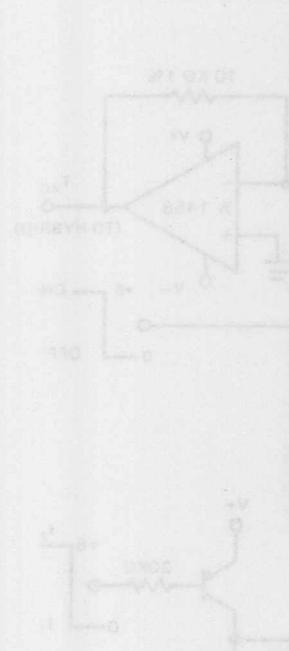
Amplitude vs. Frequency Characteristics of a C_2 Phone Line

Amplitude vs. Frequency Characteristics of a 3002/C0 Phone Line

Group Delay vs. Frequency Characteristics of a C2 Phone Line
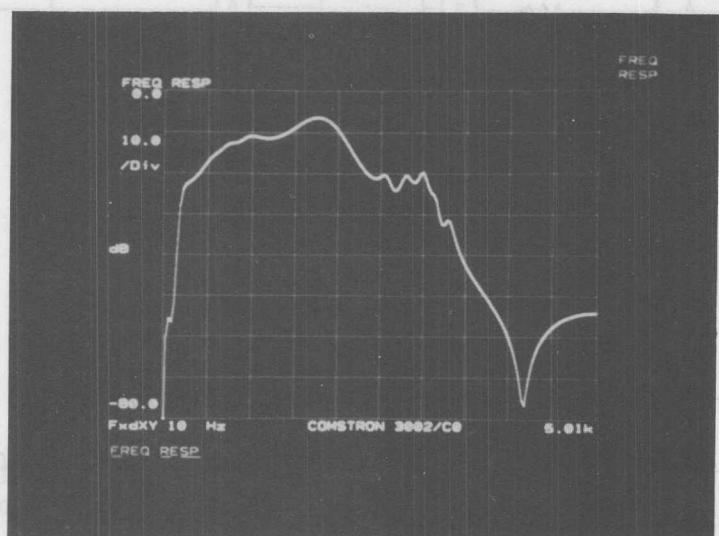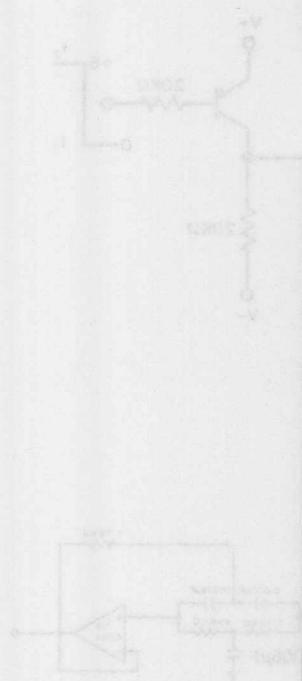
Group Delay vs. Frequency Characteristics of a 3002/C0 Phone Line

APPENDIX B
EIA RS-232-C Interface

The listing that follows contains the data, control, timing, and grounding interfaces as prescribed in EIA Standard RS-232-C. Not listed are pins 9 and 10 (reserved for testing), and pins 11, 18, and 25 (unassigned).

Pin 1. AA: Protective Ground Conductor is electrically bonded to equipment frame. Can also be connected to external grounds as required by applicable regulations.

Pin 2. BA: Transmitted Data Signals on this circuit are generated by the DTE and are transferred to the local DCE for transmission of data to remote DTE via the remote DCE. Familiarly known as Send Data (SD).

Pin 3. BB: Received Data Direction From DCE. Signals on this circuit are generated by the receiving DCE in response to data signals received from remote DTE via the remote DCE. Familiar mnemonic is RD.

Pin 4. CA: Request to Send Direction: To DCE. Signals on this circuit are used to condition the local DCE for data transmission and, on half-duplex channels, to control the direction of data transmission. Familiar mnemonic is RTS or RS.

Pin 5. CB: Clear to Send Direction: From DCE. Signals on this circuit indicate if the DCE is ready to transmit data. Familiar mnemonic is CTS or CS.

Pin 6. CC: Data Set Ready Direction: From DCE. Signals on this circuit indicate the local modem is connected to a communications channel and is not in a test mode. Familiarly known as Modem Ready (MR).

Pin 7. AB: Signal Ground The common ground reference potential for all circuits except protective ground.

Pin 8. CF: Received Line Signal Detector Direction: From DCE. Signals on this circuit indicate that a valid carrier is being received by the DCE. Familiarly known as Carrier On (CO) or Carrier Detected (CD).

Pin 12. SCF: Secondary Received Line Signal Detector Direction: From DCE. Same as CF except that carrier is being received on the secondary channel, not the primary channel.

Pin 13. SCB: Secondary Clear to Send Direction: From DCE. Same as CB except the DCE is ready to transmit data on the secondary channel, not the primary channel.

Pin 14. SBA: Secondary Transmitted Data Direction: To DCE. Same as BA except the data is transmitted on the secondary channel, not the primary channel.

Pin 15. DB: Transmitter Signal Element Timing (DCE Source) Direction: From DCE. Signals on this circuit provide the DTE with transmitted signal element timing. The on to off transitions of this signal coincide with the transitions between signal elements. Familiarly known as Transmit Clock (TXC).

Pin 16. SBB: Secondary Received Data Direction: From DCE. Same as BB except that data signals are received on the secondary channel, not the primary channel.

Pin 17. DD: Receiver Signal Element Timing (DCE Source) Direction: From DCE. Signals on this circuit provide the DTE with received signal element timing. The on to off transitions of this signal is the nominal center of the signal element. Familiarly known as Receive Clock (RXC).

Pin 19. SCA: Secondary Request to Send Direction: To DCE. Same as CA except the DCE is conditioned to transmit on the secondary channel, not the primary channel.

Pin 20. CD: Data Terminal Ready Direction: To DCE. Signals from the DTE on this circuit indicate the DTE is ready to transmit and receive data. Familiarly known as Terminal Ready (TR).

Pin 21. CG: Signal Quality Detector Direction: From DCE. Signal on this circuit from DCE indicates if there is a predefined high probability of error. When on, no errors are suspected. When off, the error probability is high.

Pin 22. CE: Ring Indicator Direction: From DCE. Signals on this circuit indicate a ringing signal is being received. Familiar mnemonic is RI.

Pin 23. CH/CI: Data Signal Rate Selector Direction: CH, to DCE; CI, from DCE. Signals on this circuit select between two data rates (synchronous systems) or two ranges of rates (asynchronous systems) for dual-rate DCE.

Pin 24. DA: Transmitter Signal Element Timing (DTE Source) Direction: To DCE. Signals on this circuit provide the DCE with transmitted signal element timing. The on to off transition of the signal is the nominal center of the signal element. Familiarly known as External Transmit Clock (XTXC).

APPENDIX C
Analog and Digital Loopback and Testing
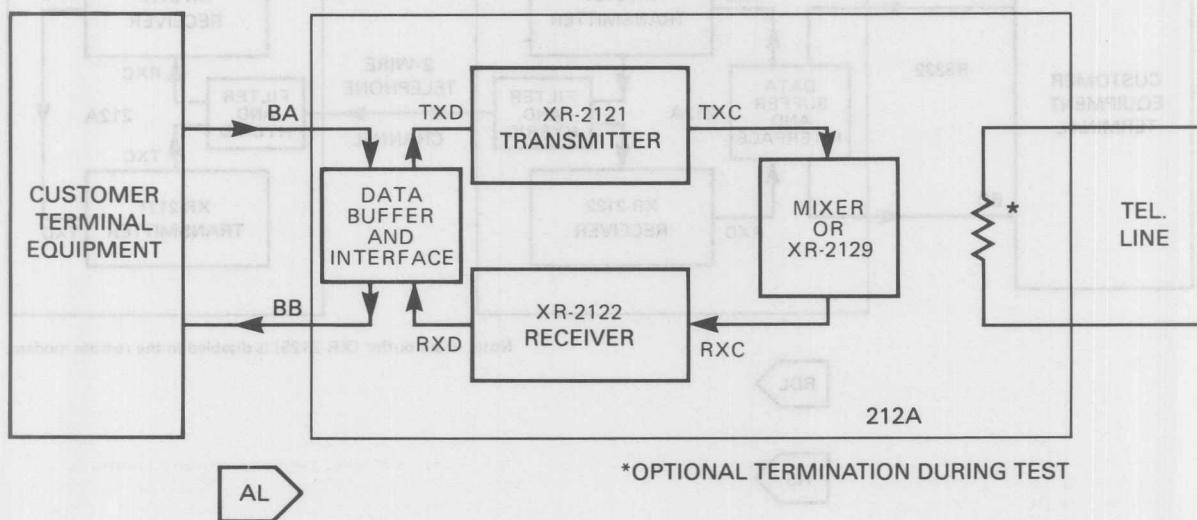
*OPTIONAL TERMINATION DURING TEST

ANALOG LOOP TEST

*OPTIONAL TERMINATION DURING TEST

SELF-TEST ANALOG LOOP

21

LOCAL

REMOTE

CUSTOMER EQUIPMENT TERMINAL

BA

RS232

BB

TXD

XR-2121 TRANSMITTER

DATA BUFFER AND INTERFACE

212A

RXD

XR-2122 RECEIVER

FILTER AND HYBRID

2-WIRE TELEPHONE CHANNEL

FILTER AND HYBRID

XR-2122 RECEIVER

RXD

RXC

212A

TXC

XR-2121 TRANSMITTER

TXD
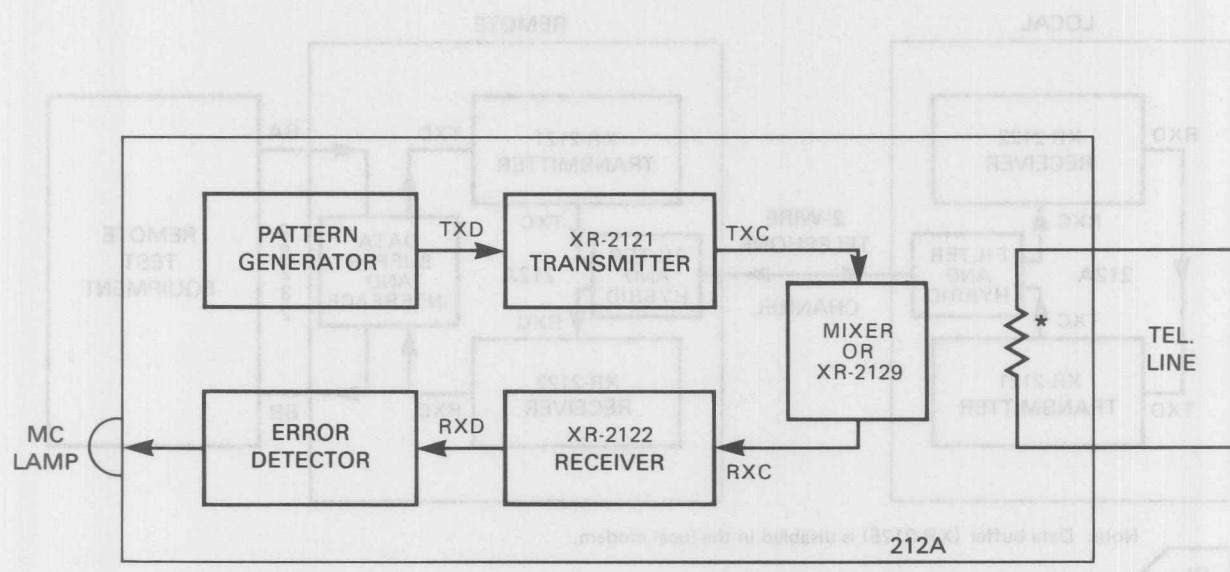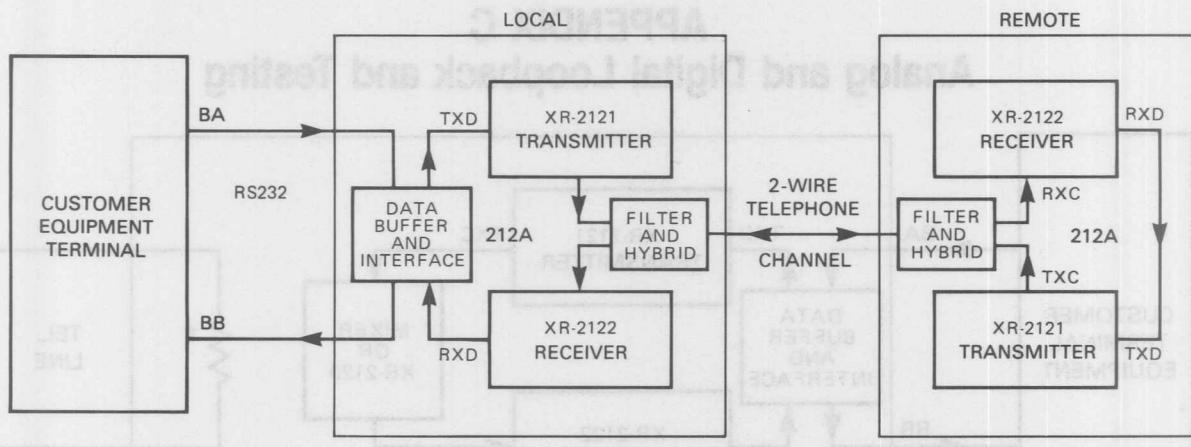
Note: Data buffer (XR-2125) is disabled in the remote modem.

RDL

HS

NOTE: HIGH SPEED ONLY

REMOTE DIGITAL LOOP

LOCAL

REMOTE

RXD

XR-2122 RECEIVER

RXC

212A

TXC

FILTER AND HYBRID

TXD

XR-2121 TRANSMITTER

2-WIRE TELEPHONE CHANNEL

FILTER AND HYBRID

XR-2121 TRANSMITTER

TXD

TXC

212A

RXC

XR-2122 RECEIVER

RXD

DATA BUFFER AND INTERFACE

BA

RS232

BB

REMOTE TEST EQUIPMENT
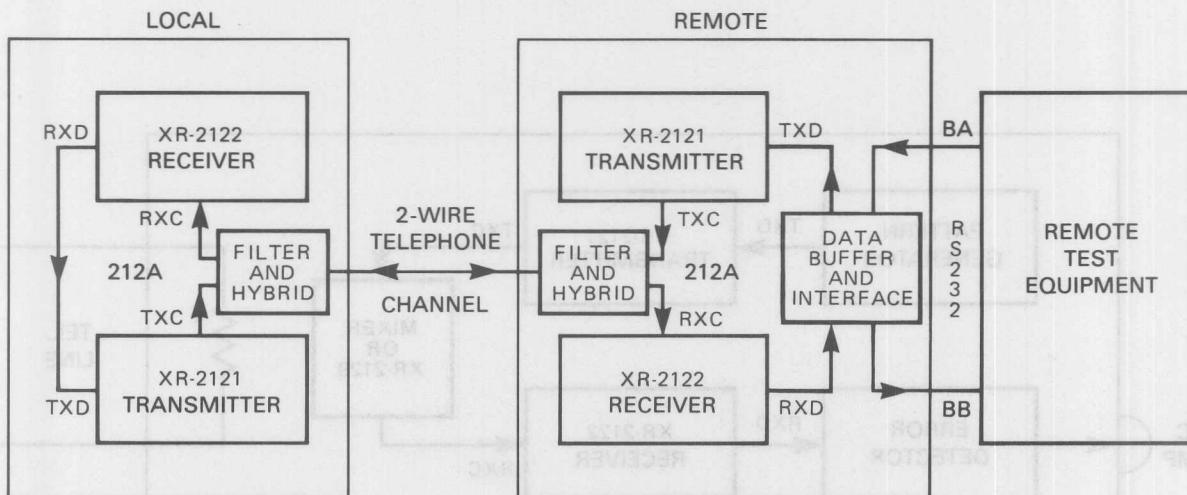
Note: Data buffer (XR-2125) is disabled in the local modem.

DL

DIGITAL LOOP

22

LOCAL

PATTERN GENERATOR → TXD → XR-2121 TRANSMITTER

212A

XR-2122 RECEIVER ← RXD

FILTER AND HYBRID

ERROR DETECTOR

MC LAMP

2-WIRE TELEPHONE CHANNEL

REMOTE

XR-2122 RECEIVER → RXD

FILTER AND HYBRID

212A

XR-2121 TRANSMITTER → TXD

Note: Data buffer (XR-2125) is disabled in the remote modem.

ST >

RDL >

HS >
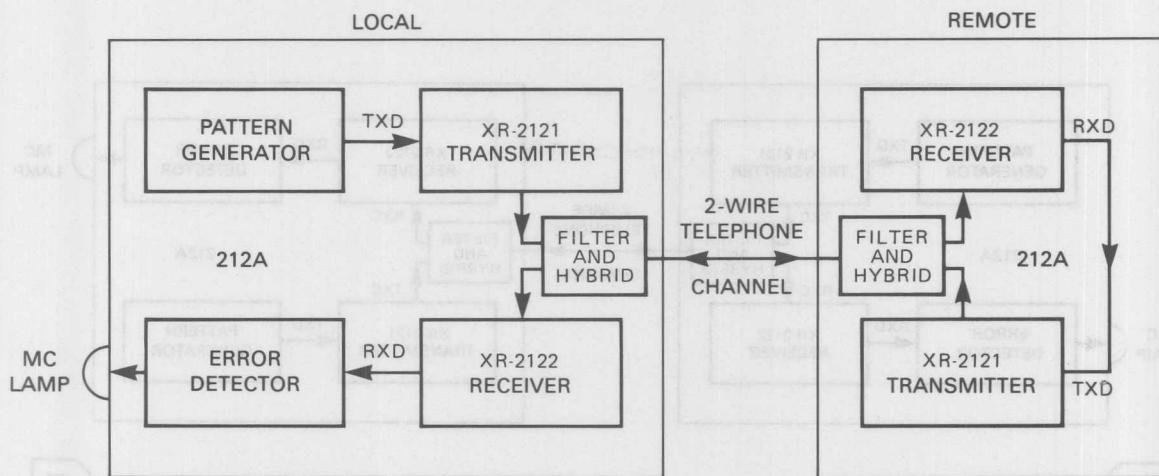
NOTE: HIGH SPEED ONLY

SELF-TEST REMOTE DIGITAL LOOP
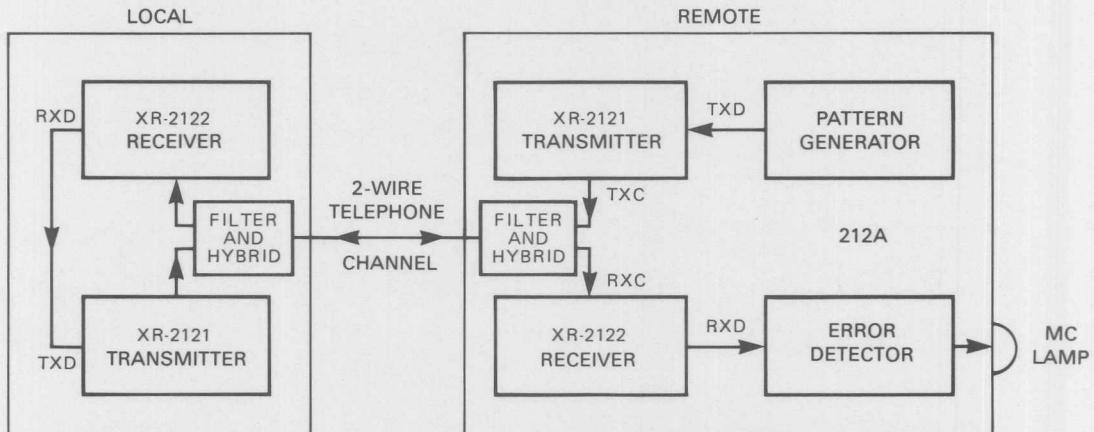
LOCAL

RXD → XR-2122 RECEIVER

FILTER AND HYBRID

XR-2121 TRANSMITTER

TXD

2-WIRE TELEPHONE CHANNEL

REMOTE

XR-2121 TRANSMITTER ← TXD ← PATTERN GENERATOR

FILTER AND HYBRID

TXC

212A

RXC

XR-2122 RECEIVER → RXD → ERROR DETECTOR → MC LAMP

DL >   Note: Data buffer (XR-2125) is disabled in the remote modem.

< ST

SELF-TEST DIGITAL LOOP

23

END TO END SELF-TEST

24
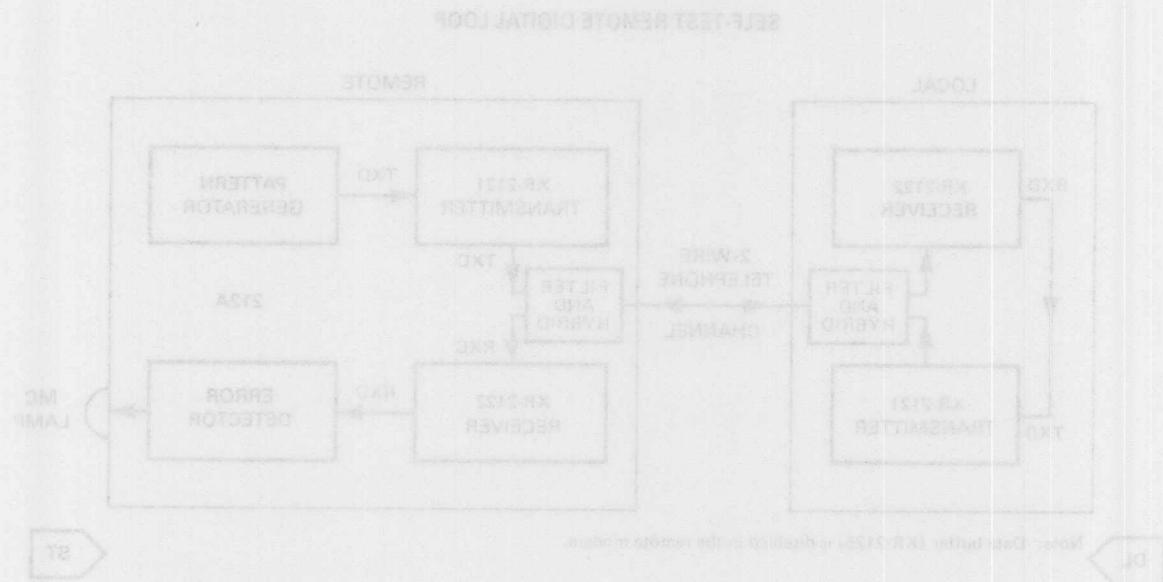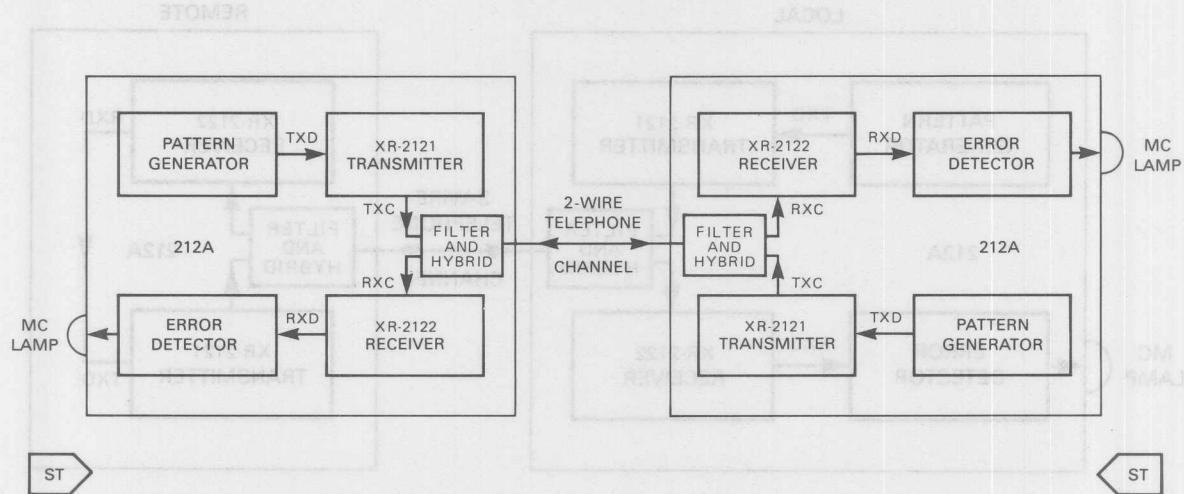
APPENDIX D
XR-212AS MSP Performance Specifications

C2 LINE
ANSWER OR
ORIGINATE MODE
1200 BPS OPERATION
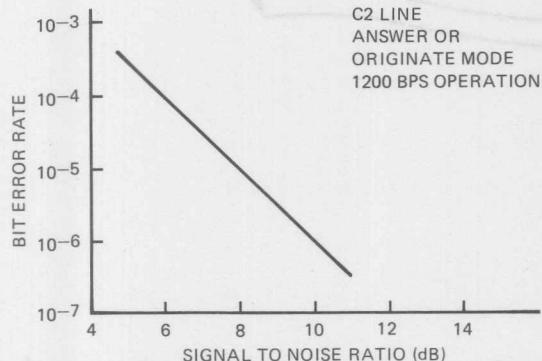
Dynamic Range:	0 dBm to −45dBm (45 db)
Frequency Offset (BER less than 10^{-5}):	± 9 Hz for C2 line ± 5 Hz for C0 or back-to-back line
Bias Distortion:	less than 5%
Jitter:	less than 8%

BACK-TO-BACK
LINE CONDITION
1200 BPS OPERATION

ORIG/ANS
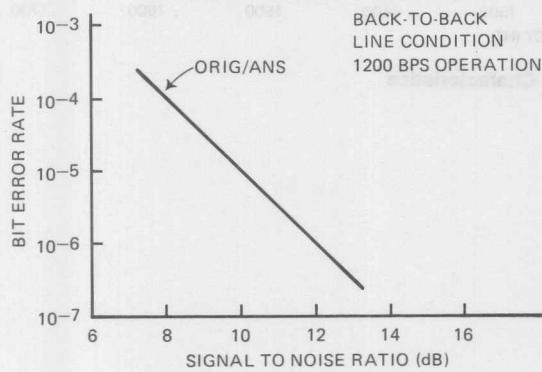
XR-212AS BER PERFORMANCE

1200 BPS OPERATION

Conditions: R_{XC} = -30 dBm, T_{XC} = -9 dBm

	S/N FOR < $1/10^{-5}$ ERRORS		
MODE	LINE C0	C2	B/B
ANS/ORIG	12 dB	8 dB	10 dB

300 BPS OPERATION

Conditions: R_{XC} = -30 dbm, T_{XC} = - 9 dBm

	S/N FOR < $1/10^{-5}$ ERRORS		
MODE	LINE C0	C2	B/B
ANS/ORIG	5 dB	7 dB	3 dB

ANS   ORIG

C0 LINE
1200 BPS OPERATION
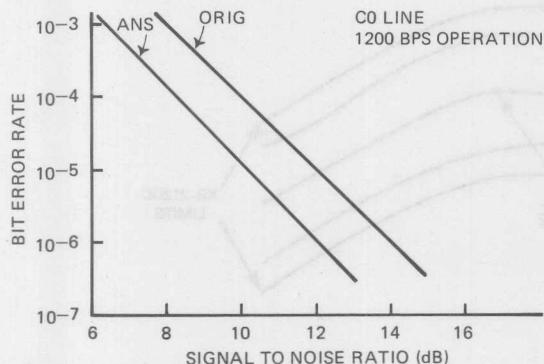
XR-212AS Bell Performance
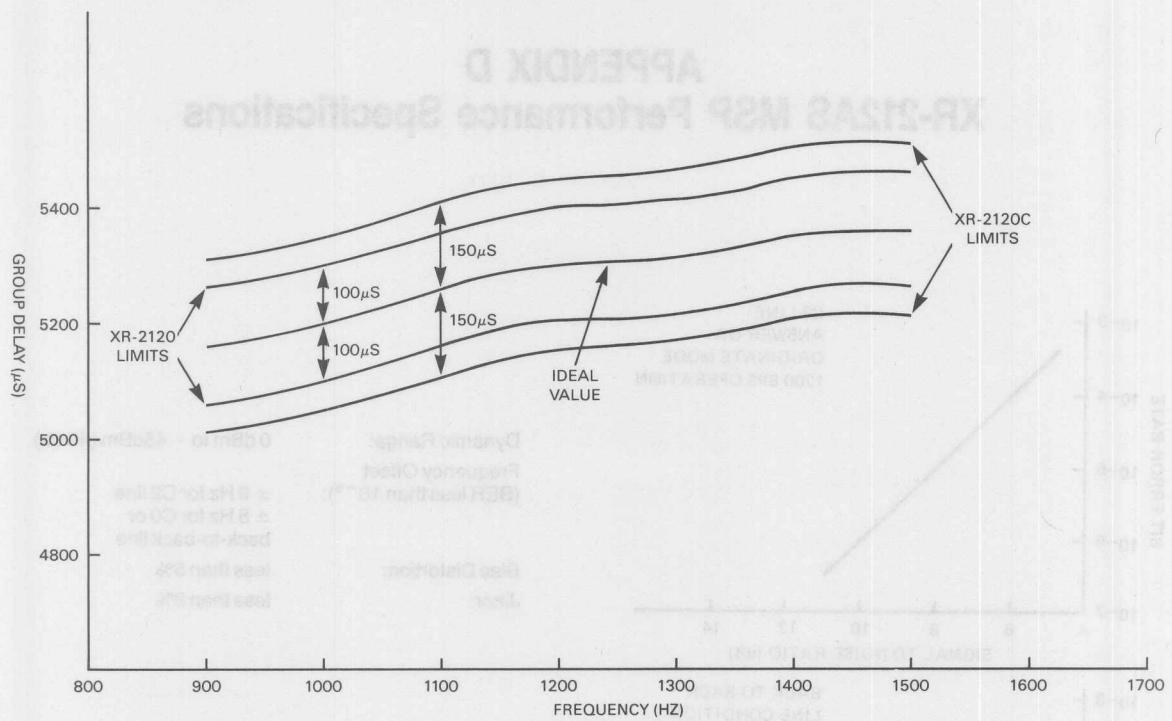
Low Band Group Delay Characteristics

High Band Group Delay Characteristics

26
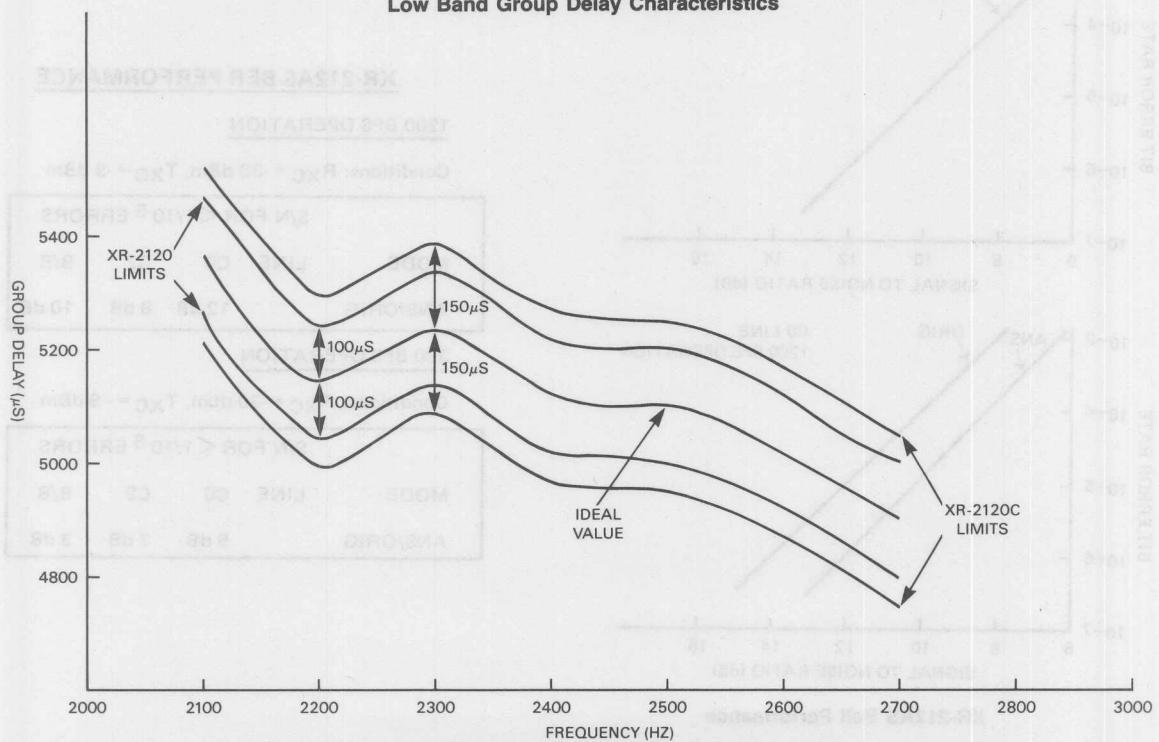
PSK Modem Filter

GENERAL DESCRIPTION

The XR-2120 is a self-contained bandpass filter set designed for realization of Bell 212A compatible 1200 bits/sec PSK modems. The XR-2120 utilizes CMOS technology and switched capacitor circuit techniques to minimize external components to a single crystal or frequency source. Contained in the device are two complete bandpass filters centered around the Bell standard 1200 Hz and 2400 Hz send and receive frequencies. These filters also provide compromise line equalization. Additional features included are digitally programmable transmit and receive gains as well as input anti-aliasing and complete output smoothing filters. Separate V_{SS} pins for transmit, receive, and digital sections are provided to minimize crosstalk.

The XR-2120 features guaranteed filter group delay specifications, within ±100μS of nominal. The XR-2120C is a relaxed version of the XR-2120 with group delay specified within ±150μS. The devices are available in a 22 pin (0.4 inch wide) plastic or ceramic package, and operate over a wide range of supply voltages.

FEATURES

On-board Crystal Oscillator With Buffered Output
Internal Anti-aliasing Filters
Complete On-board Output Active Filters
Digitally Programmable Transmit and Receive Gains
MODE Input Internally Switches Filters
    for Answer/Originate
Single or Split Supply Operation
Center Frequencies Movable with Input Clock
High-Impedance Inputs (100 kΩ min)
1% Center Frequency Accuracy
Separate CLK IN and CLK OUT Pins

APPLICATIONS

Bell 212A Transmit/Receive Filtering
Answer Back Signal Filtering

ABSOLUTE MAXIMUM RATINGS

Power Supply	16V
Power Dissipation, Plastic	1.0W
Derate Above 25°C	5 mW/°C
Power Dissipation, Ceramic	1.3W
Derate Above 25°C	7 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Any Input Voltage	$(V_{DD} + 0.5V)$ to $(V_{SS} - 0.5V)$

FUNCTIONAL BLOCK DIAGRAM
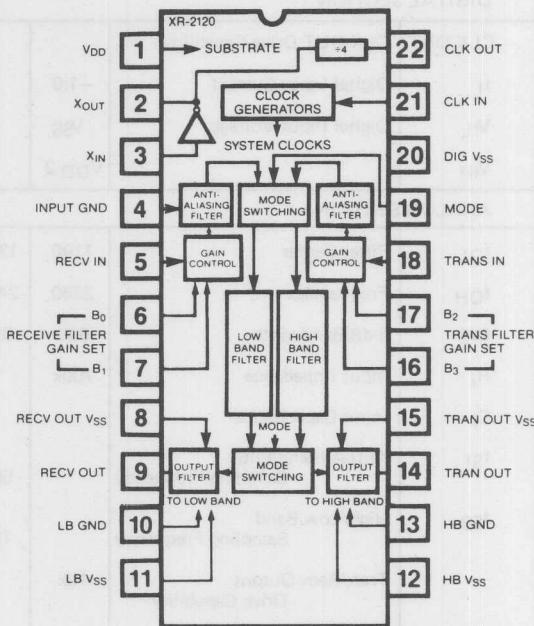
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2120CN	Ceramic	0°C to +70°C
XR-2120CP	Plastic	0°C to +70°C
XR-2120N	Ceramic	0°C to +70°C
XR-2120P	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2120 is comprised of four main signal blocks: The digitally programmable gain amplifier, an input anti-aliasing switched capacitor filter, switched capacitor bandpass filters at 1200 Hz and 2400 Hz, and output RC active filters. These sections serve to: (1) amplify and condition incoming signals, (2) remove noise which can cause aliasing problems in the bandpass filters, (3) provide very precise bandpass filtering and phase compensation, and (4) perform output reconstruction and filtering. To perform these necessary filtering and phase compensation functions, a total of 48 poles are used in the XR-2120.

The programmable gain stages provide 4 selectable gains for transmit or receive. Separate clock output and input pins are provided for flexibility.

XR-2120

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V, V_{SS} = −5 V, X_{IN} = 4.032 MHz (CLK IN = 1.008 MHz), T_A = 25°C, unless otherwise specified. Input gain = 0 dB (B1/B3 = B0/B2 = 0).

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DIGITAL SECTION						
CLK OUT	CLK OUT Drive Capability			50	pF	
I_I	Digital Input Current	−1.0		1.0	µA dc	
V_{IL}	Digital Input Voltage	V_{SS}		V_{SS}+2	V	For "0" Level
V_{IH}		V_{DD}-2		V_{DD}	V	For "1" Level
ANALOG SECTION						
f_{OL}	Filter Center	1190	1200	1210	Hz	Low Band
f_{OH}	Frequencies	2380	2400	2420	Hz	High Band
BW	3 dB Bandwidth	900	950		Hz	Either Band
R_i	Input Impedance	100k			Ohms	
C_i	Input Capacitance			10	pF	
f_{SI}	Anti-Aliasing Filter Sampling Frequency		504		kHz	
f_{SB}	High/Low Band Sampling Frequency		126		kHz	
	Tran/Recv Output Drive Capability	10k		50	Ohms pF	
	Output Clock Feedthrough			2	mV rms	at 126 kHz
e_O100	Output Noise		160		µV rms	In Passbands (100 Hz BW)
e_O1000	Output Noise		700		µVrms	In Passbands (1kHz BW)
ei_{range}	Dynamic Range of Filters		70		dB	Note 1
Vo_{SW}	Output Voltage Swing	6.0	6.8		V pp	Note 2
2ndHarm	2nd Harmonic Content		-60		dB	f_{IN} = 1200 Hz Referenced to Fundamental
T_{SW}	Mode Switching		10		ms	
I_{DD}	Supply Current		9	27	mA	
V_{SUP}	Supply Voltage Range	±4.75 9.5	±5 10	±7.5 15.0	V V	Dual Supplies V_{DD} Reference to V_{SS}
A_V	Passband Gain Low Band	3.2 −1.4	4.2 0	5.2 1.4	dB dB	Input Gain = 0 dB 1200 Hz 900 - 1500 Hz (Note 3)
	High Band	2.8 −1.7 0	3.8 0 1.2	4.8 1.7 2.2	dB dB dB	2400 Hz 2100 - 2500 Hz (Note 3) 2500 - 2800 Hz (Note 3)

Note 1 Dynamic range is defined as ei_{range} = 20 Log (Vo_{SW}/e_O).
Note 2 Vo_{SW} is the maximum output swing before output clipping occurs.
Note 3 Gain measurements are relative to passband center frequency gain normalized to 0 dB.

28

XR-2120

ELECTRICAL CHARACTERISTICS Continued

FILTER RESPONSE

SYMBOL	PARAMETER	XR-2120			XR-2120C			UNIT	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
GD	Group Delay								
	Low Band Filter	5060	5160	5260	5010	5160	5310	μs	900 Hz (See Figure 7)
		5100	5200	5300	5050	5200	5350	μs	1kHz
		5160	5260	5360	5110	5260	5410	μs	1.1kHz
		5200	5300	5400	5150	5300	5450	μs	1.2kHz
		5215	5315	5415	5165	5315	5465	μs	1.3kHz
		5255	5355	5455	5205	5355	5505	μs	1.4kHz
		5260	5360	5460	5210	5360	5510	μs	1.5kHz
	High Band Filter	5270	5370	5470	5220	5370	5520	μs	2.1kHz (See Figure 8)
		5040	5140	5240	4990	5140	5290	μs	2.2kHz
		5140	5240	5340	5090	5240	5390	μs	2.3kHz
		5015	5115	5215	4965	5115	5265	μs	2.4kHz
		5000	5100	5200	4950	5100	5250	μs	2.5kHz
		4920	5020	5120	4870	5020	5170	μs	2.6kHz
		4800	4900	5000	4750	4900	5050	μs	2.7kHz

EQUIVALENT SCHEMATIC DIAGRAM
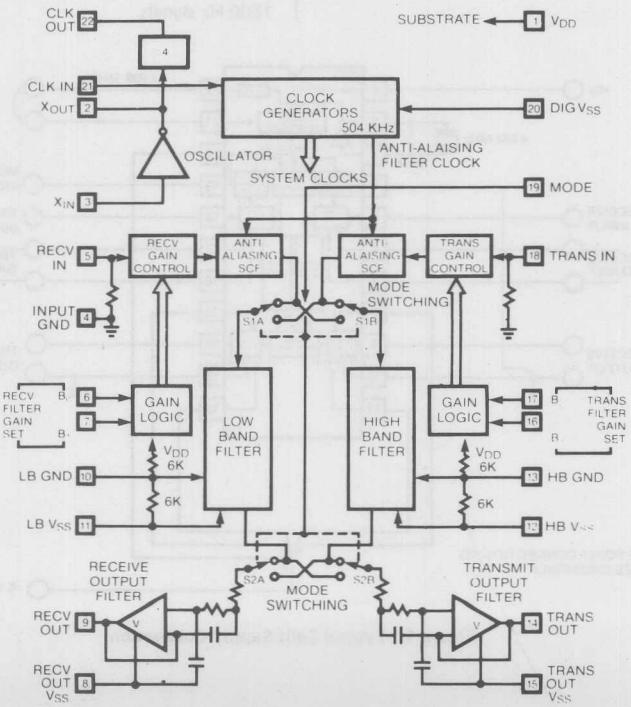
XR-2120

PRINCIPLES OF OPERATION

Figure 1 shows the typical connection for the XR-2120 in a split supply configuration. In this mode, Pins 4, 10, and 13, are simply tied to ground. For single supply operation, Pins 10 and 13 internally bias to half supply and should be externally bypassed with 2.2 μF capacitors. Pin 4 does not internally dc bias, however, Pin 10 or 13 can provide it with a half supply bias point. In this connection, a 10 kΩ resistor should be used between Pin 4, and Pin 10 or 13, with Pin 4 bypassed with a 2.2 μF capacitor.

Signal flow is illustrated as shown in Figure 2. The transmit or receive signal will follow a path through four internal blocks. First it passes through a digitally programmable gain stage. The gain, as a function of a 2-Bit digital input, is shown in Figure 3. Next, the signal passes through a two-pole anti-aliasing low-pass filter at 12 kHz. This is used to remove noise around the main filter switching frequency of 126 kHz. The anti-aliasing filter is also a sampled-data filter, but is switched at a much higher rate of 504 kHz. It is necessary, therefore, to ensure that wideband noise above 252 kHz is not present at the inputs. In noisy environments a single noise pole RC filter at 30 kHz is usually sufficient for filtering input noise. The third signal block is the main bandpass filtering section at 1200 Hz or 2400 Hz, depending on the mode selected. The last section is the output

smoothing filter; a two-pole RC active filter used to reconstruct the signal from its sampled data form.

The mode input pin is used to direct the transmit and receive signals to the appropriate filter section. Figure 4 shows mode selection logic convention.

The XR-2120 is designed to be operated with a 4.032 MHz crystal between the X_{IN} and X_{OUT} pins. The 4.032 MHz is divided by four and output on the CLK OUT pin, Pin 22. For normal operation, the CLK OUT is tied to the CLK IN pin, Pin 21; however, the bandpass center frequencies can be decreased by providing a divider between these two pins. An external CLK can be used by inputing a 1.008 MHz clock into the CLK IN pin, or a 4.032 MHz clock into the X_{IN} pin.

Figure 5 shows circuitry suitable for translating TTL signals to the CMOS levels required by all XR-2120 digital inputs. The amplitude and group delay characteristics of the XR-2120 are shown in Figures 6 through 8.

The XR-2120 may also be used in CCITT V.22 applications by adding guard tone notch filters as shown in Figure 9 or 10. This type of filter, when used with the XR-2120, will produce at least 60 dB of attenuation to either 550 Hz or 1800 Hz signals.


*SINGLE POINT CONNECTION TO MINIMIZE CROSSTALK
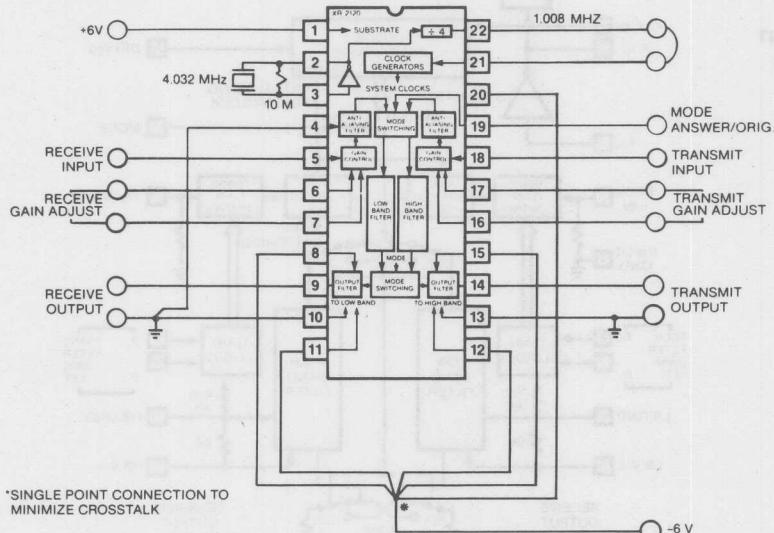
Figure 1: Typical Split Supply Connection.
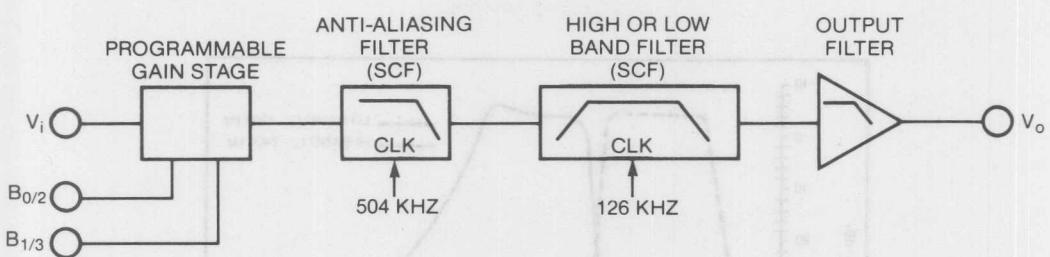
Figure 2: Signal Path

B1 / B3	B0 / B2	INPUT GAIN (dB)
0	0	0
0	1	6
1	0	10
1	1	14

1 = Logic High
0 = Logic Low

Figure 3: Gain Programming (Nominal Gain Shown in Fig. 6)

MODE PIN	TRANSMIT	RECEIVE	TERMINOLOGY
1	Low Band	High Band	Originate
0	High Band	Low Band	Answer

Figure 4: Mode Selection Logic

(A) SINGLE SUPPLY

(B) SPLIT SUPPLY
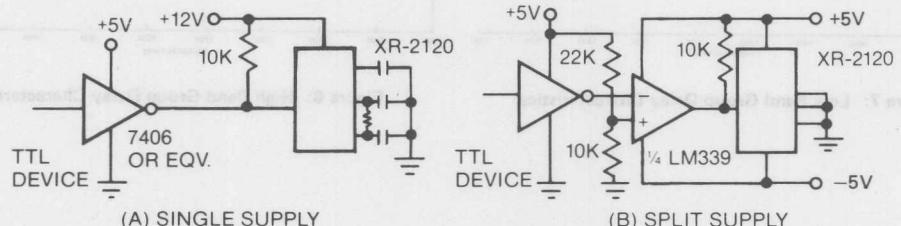
Figure 5: TTL Interfacing of Digital Inputs.
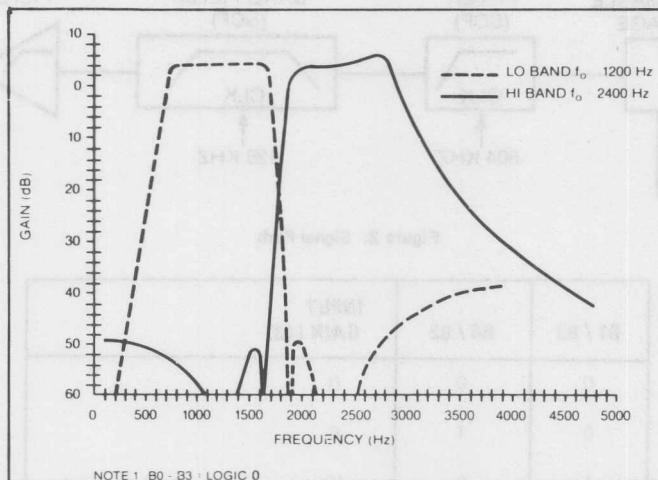
Figure 6: High and Low Band Amplitude Response.
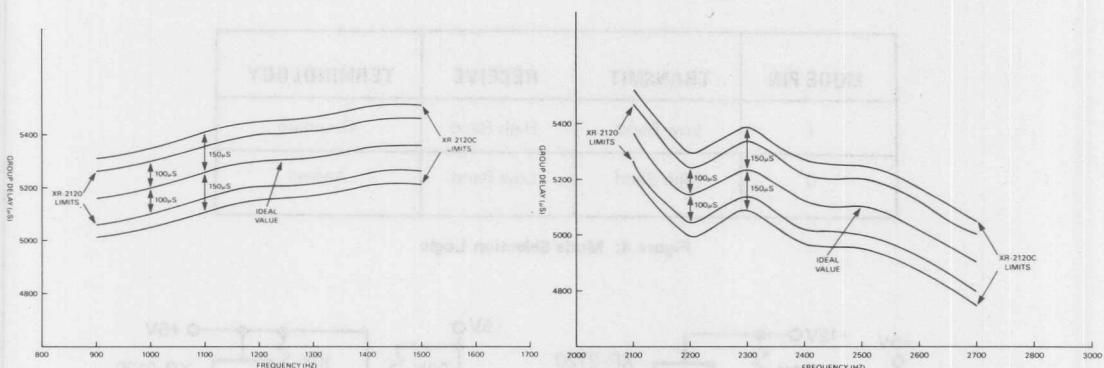
Figure 7: Low Band Group Delay Characteristics
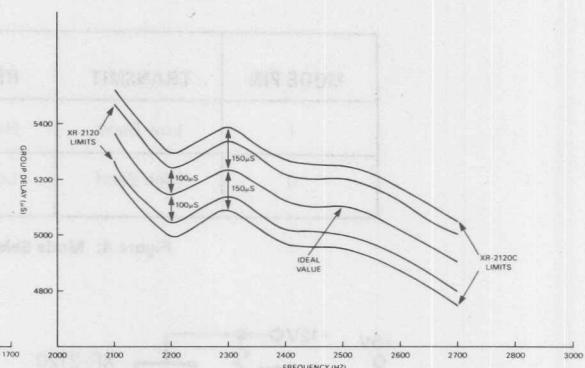
Figure 8: High Band Group Delay Characteristics
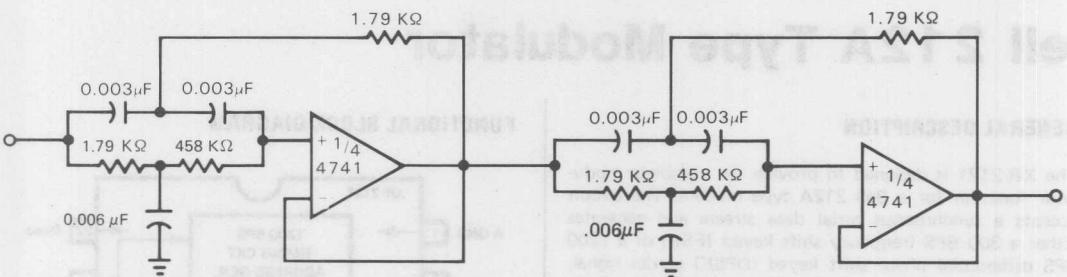
**Figure 9. V.22 1800 Hz Notch Filter**
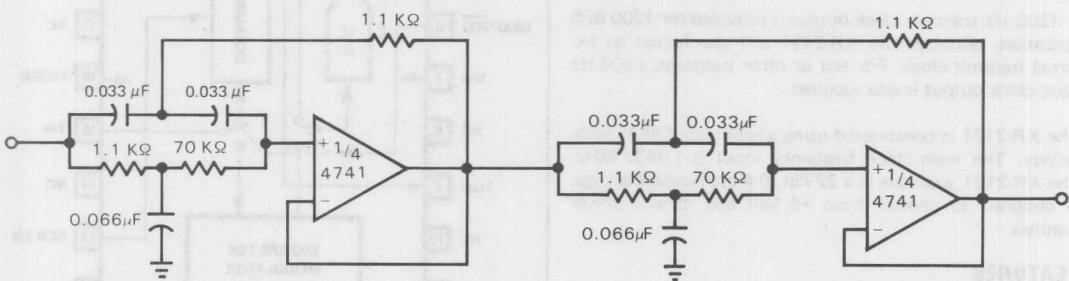
Figure 10. V.22 550 Hz Notch Filter

Bell 212A Type Modulator

GENERAL DESCRIPTION

The XR-2121 is designed to provide the complete modulator function for a Bell 212A type modem. The circuit accepts a synchronous serial data stream and generates either a 300 BPS frequency shift keyed (FSK) or a 1200 BPS differential phase shift keyed (DPSK) carrier signal. An on-board digital-to-analog converter provides a synthesized sine wave output. Also provided on the transmitted carrier output is an inverting amplifier with external feedback resistor to provide a carrier amplitude adjust.

The XR-2121 contains an internal 17 bit scrambler. This scrambler which is used during DPSK operation has a disable input for sending non-scrambled carriers.

A 1200 Hz transmit clock output is provided for 1200 BPS operation, although the XR-2121 will also accept an external transmit clock. For test or other purposes, a 600 Hz baud clock output is also supplied.

The XR-2121 is constructed using silicon gate CMOS technology. The main clock frequency input is 1.8432 MHz. The XR-2121, available in a 22 Pin (0.4 inch wide) package, is designed to operate from +5 volt and -5 volt power supplies.

FEATURES

Bell 212A Compatible
1200 BPS DPSK
300 BPS FSK
Digital Modulation Techniques for DPSK
External Transmit Clock Input
600 Hz Dibit Clock Output
Complete Scrambler Function with Disable Input
Transmit Carrier Level Adjust
1.8432 MHz Clock
±5 Volt Operation

APPLICATIONS

Bell 212A Type Modulator
Bell 103 Type Modulator

ABSOLUTE MAXIMUM RATINGS

Power Supply
V_{DD} — -0.3 to +7V
V_{SS} — +0.3 to -7V
Input Voltage — V_{SS} -0.3V to V_{DD} +0.3V
DC Input Current — ±10 mA
Power Dissipation — 1.0 W
Derate Above 25°C — 5 mW/°C
Storage Temperature Range — -65°C to +125°C

FUNCTIONAL BLOCK DIAGRAM
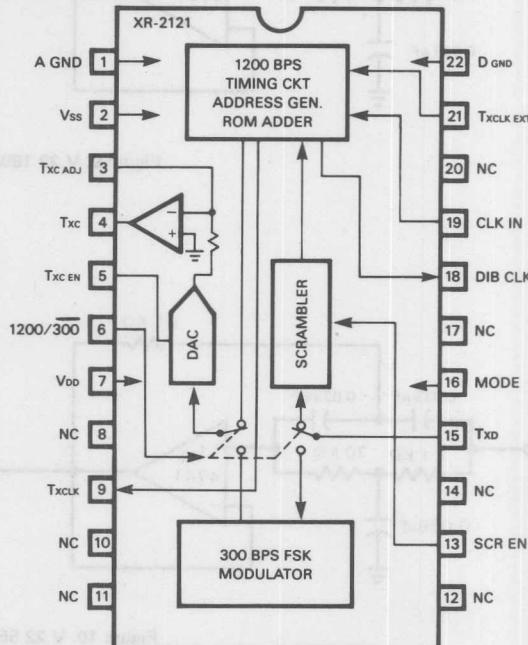
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2121CN	Ceramic	0°C to 70°C
XR-2121CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2121 basically has two types of operation, 1200 BPS DPSK or 300 BPS FSK. For 1200 DPSK the XR-2121 generates carrier frequencies of 1200 Hz or 2400 Hz, depending on mode selection (originate or answer). The carrier frequencies are imposed with phase shifts to carry the data to be transmitted (T_{XD}) over the telephone network. The phase shifts correspond to the incoming data grouped in pairs (dibits) and are one of four values — 0°, 90°, −90°, 180°

During 300 BPS FSK operation, the XR-2121 generates one of two pairs of frequencies to represent the T_{XD}. These pairs are either 1070 Hz/1270 Hz or 2025 Hz/2225 Hz depending on mode selection.

XR-2121

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V ±5%, V_{SS} = -5 V ±5%, CLK IN = 1.8432 MHz ±0.01%, T_A = 0°-70°C unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{DD}	Positive Supply Current		2.5	4	mA	
I_{SS}	Negative Supply Current		-1.5	-2.5	mA	
DIGITAL INPUTS/OUTPUTS						
V_{OH}	Output High Voltage	2.4			V	I_O = 1 mA
V_{OL}	Output Low Voltage		0.4	0.8	V	I_O = -1.5 mA
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{OH}	Output Drive Current	0.5	1.5		mA	V_{OH} = 3.5 V
I_{OL}	Output Drive Current	2.0	4.0		mA	V_{OL} = 0.5 V
I_{IN}	Input Current			10	μA	
ANALOG SECTION						
V_{TXC}	Transmit Carrier Amplitude		-4		dBM	R_{EXT} = 10k
V_{TXC2H}	Transmit Carrier Amplitude 2nd Harmonic Content		-40		dB	$R_L \geqslant$ 10k
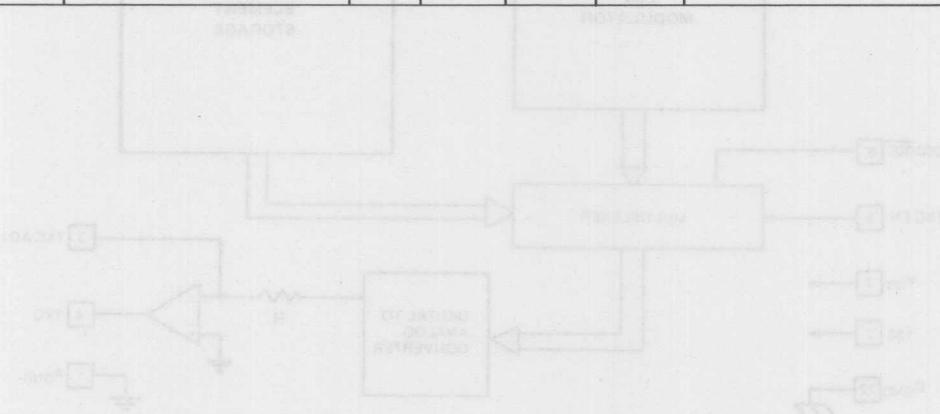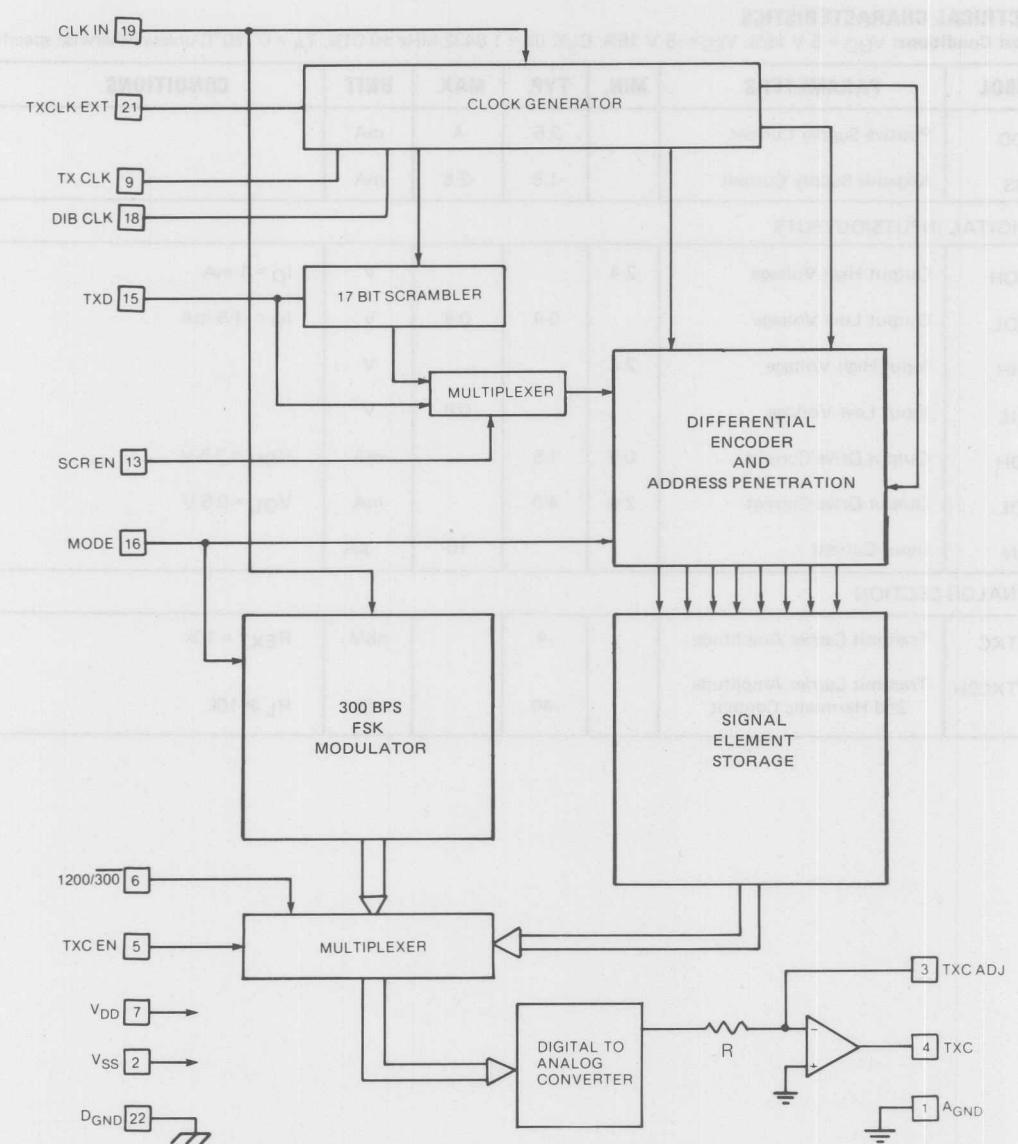
EQUIVALENT SCHEMATIC DIAGRAM

XR-2121

PRINCIPLES OF OPERATION

The XR-2121 is designed to perform all the necessary functions for the modulator section of a Bell 212A type modem. It has been specifically designed to operate with the XR-2120 filter, XR-2122 demodulator, and XR-2125 data buffer to form the complete Bell 212A type modem signal processor. This data sheet will cover just the XR-2121 and its functions with Application Note AN-28 covering the complete system.

The XR-2121 has two basic types of operation; that of a 1200 BPS differential phase shift keyed (DPSK) or 300 BPS frequency shift keyed (FSK) modulator.

The 1200 BPS section of the XR-2121 converts a serial synchronous data stream (T_{XD}) into a DPSK encoded carrier suited for transmission over a standard telephone switched network. The incoming data, T_{XD}, is clocked into the XR-2121 by either an internally generated transmit clock, T_X CLK, or an externally applied clock, T_X CLK EXT. The internal T_X CLK is derived from the main 1.8432 MHz clock, and is precisely 1200 Hz. If an external transmit clock is applied to the T_X CLK EXT input, T_X CLK will become phase locked to T_X CLK EXT. Figure 1 shows the relationship between T_{XD} and T_X CLK (1A) and T_X CLK and T_X CLK EXT (1B).

A 1 T_{XD} AND $\overline{T_{XCLK}}$ RELATIONSHIPS

B 1 $\overline{T_{XCLK}}$ AND $\overline{T_{XCLK\ EXT}}$ RELATIONSHIPS
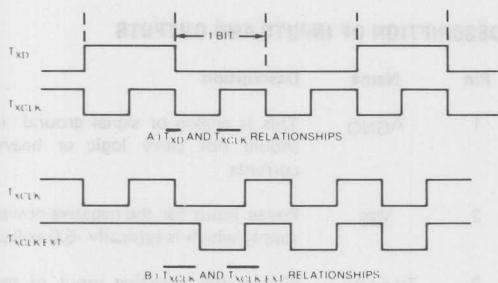
Figure 1. Transmit Data & Clock Relationships

As seen in Figure 1, data is clocked into the XR-2121 on the falling edge of T_X CLK.

1200 BPS data entering the XR-2121 is passed through a scrambler circuit, as shown in Figure 2.
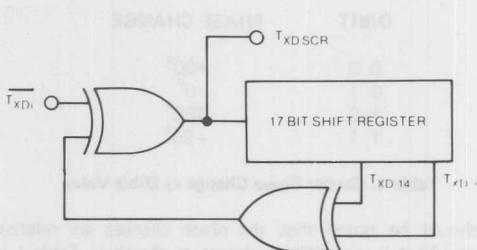
Figure 2. 17 Bit Psuedo Random Scrambler

The output of the scrambler produces a psuedo-random output which can be described by the following equation:

$$T_{XD}\ SCR = T_{XDI} \oplus T_{XD}-14 \oplus T_{XD}-17$$

$\oplus$ = exclusive − or operation

The main purpose of the scrambler is to assure that the transmitted carrier will not have extended periods of $0°$ phase shifts. This condition would cause the receiving modem's demodulator to loose lock and be unable to extract clock information from the received carrier. This condition is discussed further within the XR-2122 data sheet.

The scrambled data is fed into the actual modulator section of the XR-2121. This section phase encodes a constant frequency carrier to represent the incoming serial data, T_{XD}.* This type of phase encoding phase shift the carrier every two data bits. Figure 3 shows the relationship between the transmitted data, its clock, and the resultant phase encoded carrier. As seen in this figure, although the data rate is 1200 BPS, the baud rate is only 600. This is because phase changes only occur every two data bits or dibits. Table 1 gives the phase changes for the four possible dibit values.

*The transmit carrier frequencies for 1200 BPS operation are either 1200 Hz for originate mode or 2400 Hz for answer mode.
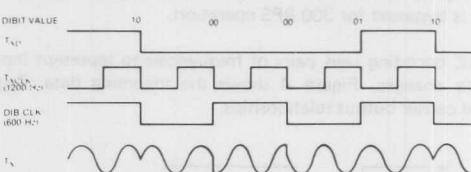
Figure 3. T_X CLK/$\overline{T_{XC}}$ Timing

DIBIT	PHASE CHANGE
0 0	+90°
0 1	0°
1 0	180°
1 1	−90°

Table 1. Carrier Phase Change vs Dibit Value

It should be noted that the phase changes are relative values. That is, each phase change as shown in Table 1 is relative to the previous carrier phase.

Figure 3 shows the T_{XC} being phase shifted, however, the XR-2121 does not introduce abrupt changes as shown there. This figure was drawn in this fashion for clarity. The XR-2121 uses digital echo modulation techniques. This technique allows incremental or slowly changing phase changes. Using this method also allows precise shaping of the frequency spectrum. The spectrum analyzer photograph in Figure 4 shows the carrier spectrum for each carrier frequency. It can be seen from the photo that separation of about 40 dB between the two spectrums is possible even before bandpass filtering. The frequency spectrums are designed for square root raised cosine shaping.
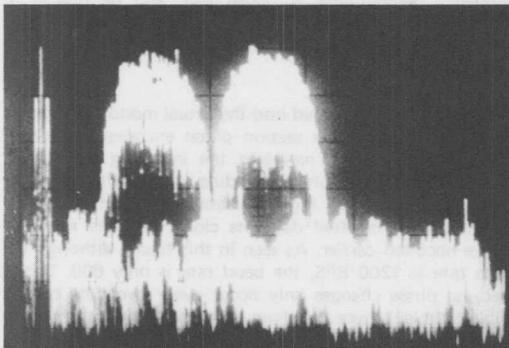

Figure 4. Transmit Carrier Spectrum

For 300 BPS operation frequency shift keying, FSK, encoding techniques are used. For this operation bit asynchronous serial data is fed into the XR-2121 data input. Being asynchronous, no transmit clock is used. The scrambler is bypassed for 300 BPS operation.

FSK encoding uses pairs of frequencies to represent input data changes. Figure 4 shows the incoming data, T_{XD}, and carrier output relationships.
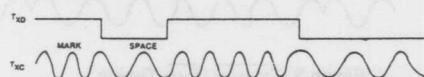

Figure 5. FSK Data Carrier Relationships

The pairs of frequencies used for the two different modes are shown in Table 2. The higher frequency in each pair is known as the mark frequency with lower the space.

MODE	CARRIER FREQUENCIES (MARK/SPACE)
Answer	2225 Hz/2025 Hz
Originate	1270 Hz/1070 Hz

Table 2. FSK Carrier Frequencies

Unlike 1200 BPS operation, for 300 BPS, the baud rate is the same as the data rate, 300. This is of course because every input data change causes a carrier frequency shift.

The outputs of both 1200 BPS and 300 BPS sections are fed into a multiplexer which routes the proper one to the output section depending on speed selection. The output circuitry consists of a seven bit digital-to-analog converter (DAC) and an output operational amplifier. The op amp is configured as an inverting amplifier with the DAC feeding an input resistor and the feedback resistor placed externally. This allows T_{XC} amplitude adjustment at this point. Pin 5, T_{XC} EN, can be used to disable transmission if desired.

DESCRIPTION OF INPUTS AND OUTPUTS

Pin	Name	Description
1	A_{GND}	This is analog or signal ground. It should not carry logic or heavy currents.
2	V_{SS}	Power input for the negative power supply which is typically -5.0 volts.
3	$T_{X}CADJ$	This is the inverting input of the output op amp. A resistor (R_{EXT}) from this pin to pin 4 (T_{XC}) sets the output amplitude of the T_{XC} (see Figure 6).
4	T_{XC}	This is the transmit carrier output.
6	1200/$\overline{300}$	Speed select input to set either 1200 BPS DPSK or 300 BPS FSK operation.
7	V_{DD}	Power input for the positive power supply which is typically +5.0 volts.
9	T_{XCLK}	The transmit clock is output on this pin. It is internally generated from the main clock input (pin 19) and is used internally to clock T_{XD} into the XR-2121.

XR-2121

13	SCR EN	The data scrambler can be enabled or disabled by this pin during 1200 BPS operation.
15	$\overline{T_{XD}}$	This is the serial data input.
16	MODE	Answer or originate modes are selected by this pin.
18	DIB CLK	The 600 Hz dibit clock is output on this pin. It may be used during system testing such as digital loopback to provide an alternating 1010... data pattern.
19	CLK IN	This is the main clock input and should be 1.8432 MHz ±0.01%.
21	$\overline{T_{X}CLK\ EXT}$	An external transmit clock may be applied to this input during 1200 BPS operation ∓0.01%.
22	D_{GND}	This is the ground for the logic circuitry of the XR-2121.

CONTROL INPUTS

Table 3 gives logic conditions for the various control inputs of the XR-2121.

| | | FUNCTION | |
PIN	NAME	LOGIC HIGH	LOGIC LOW
5	T_{XC} EN	Carrier Enabled	Carrier Disabled
6	1200/$\overline{300}$	1200 BPS Operation	300 BPS Operation
13	SCR EN	Scrambler Enabled	Scrambler Disabled
16	MODE	Answer	Originate

Table 3. Control Input Conditions

APPLICATIONS

A typical connection of the XR-2121 is shown in Figure 6.

$$T_{XC} = 20\ LOG\ (.63)(\frac{R_{EXT}}{10K})$$

$$T_X = -4\ dBM\ for\ R_{EX} = 10K$$

* => SINGLE POINT GROUND
C_1 = > 2.2μF
C_2 = > 0.01μF
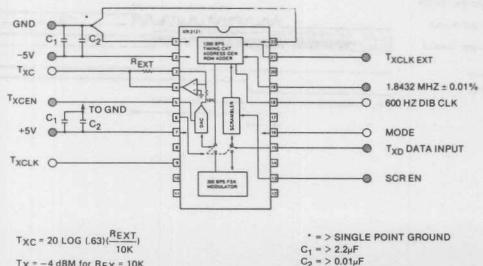
Figure 6. XR-2121 Typical Connection

The synchronous data stream is fed into T_{XD} with the T_{XC} output being either a DPSK or FSK encoded carrier. In a complete system the T_{XC} would go to the transmit filter input. Application Note AN-28 shows the XR-2121 in a complete modem signal processor.

Several output waveforms have been included to help understand the XR-2121 operation. Figure 6 shows frequency spectrums for FSK for both answer and originate modes. It can be seen to consist of two 300 Hz wide spectrums centered around 1170 Hz and 2125 Hz. Figure 7 and 8 show the higher harmonic contents of the FSK spectrums. These figures show the second harmonic content to be more than 50 dB down from the fundamental. This is very desirable in the originate mode as second harmonics not attenuated by the transmit filter will pass unattenuated through the receive and cause degraded performance.
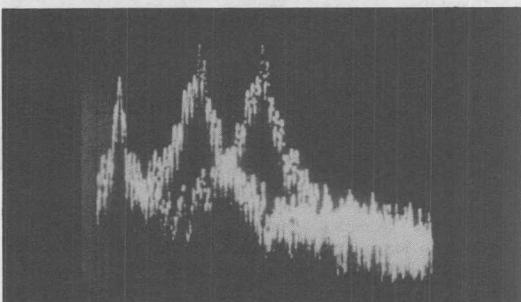
Figure 7.
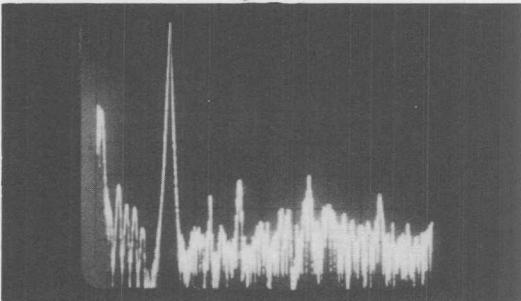
Figure 8.
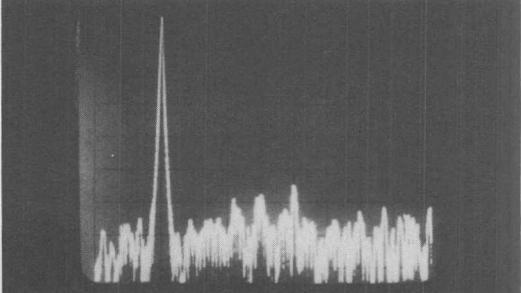
Figure 9.

Figure 9 and 10 show the carrier being enabled and disabled using the $T_{XC\ EN}$ pin (pin 5) for PSK and FSK respectively. It shows about 10 ms necessary for the carrier to be either fully enabled and settled, or disabled. These photos were taken with a transmit filter similar to the XR-2120 at the output of the XR-2121 to produce a clearer picture.
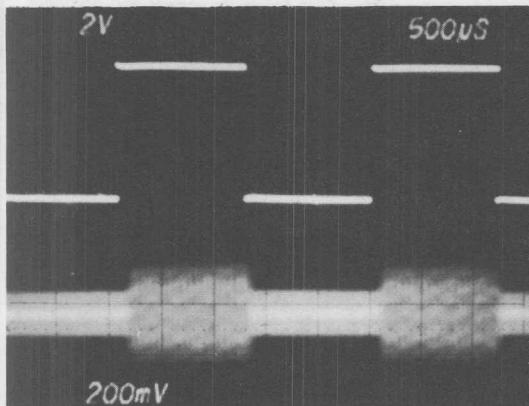
Figure 10.

For further application information on the XR-2121, Application Note AN-28 shows a complete modem signal processor utilizing the XR-2121 with the XR-2120 filter, XR-2122 demodulator, and XR-2125 data buffer.

Bell 212A Handshake

The Bell 212A modem specifications require auto speed selection on auto answer modems. Auto speed selection requires detection and decoding of the Bell 212A handshake protocol. This detection and decoding is automatically performed by the XR-2122, Bell 212A type demodulator. Some additional logic / circuitry is required to perform the handshake properly. This logic / circuitry may be digital, analog, or microprocessor-based.

Figure 12A and 12B illustrates the timing requirements for the Bell 212A handshake.
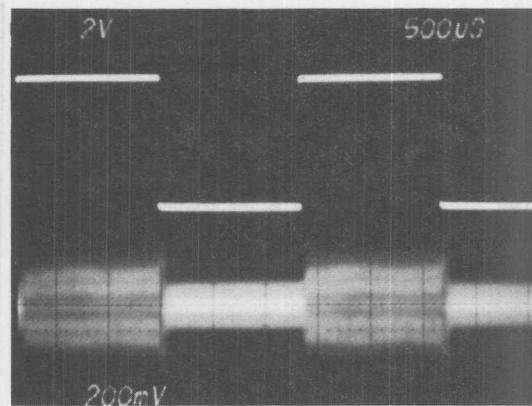
Figure 11.
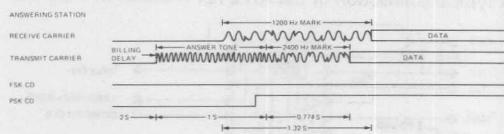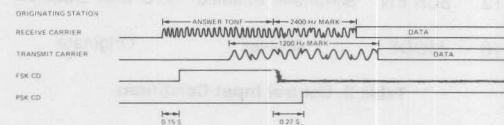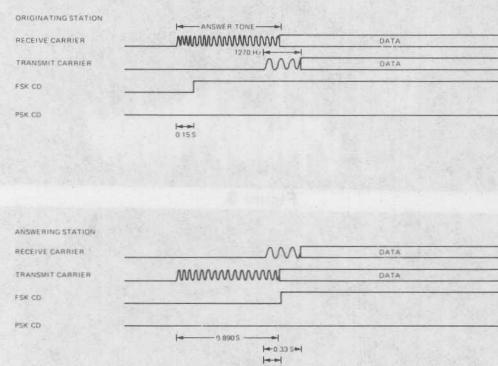
Figure 12A. Figure 12B. V.22 Handshake (with V.25 Auto Answer)
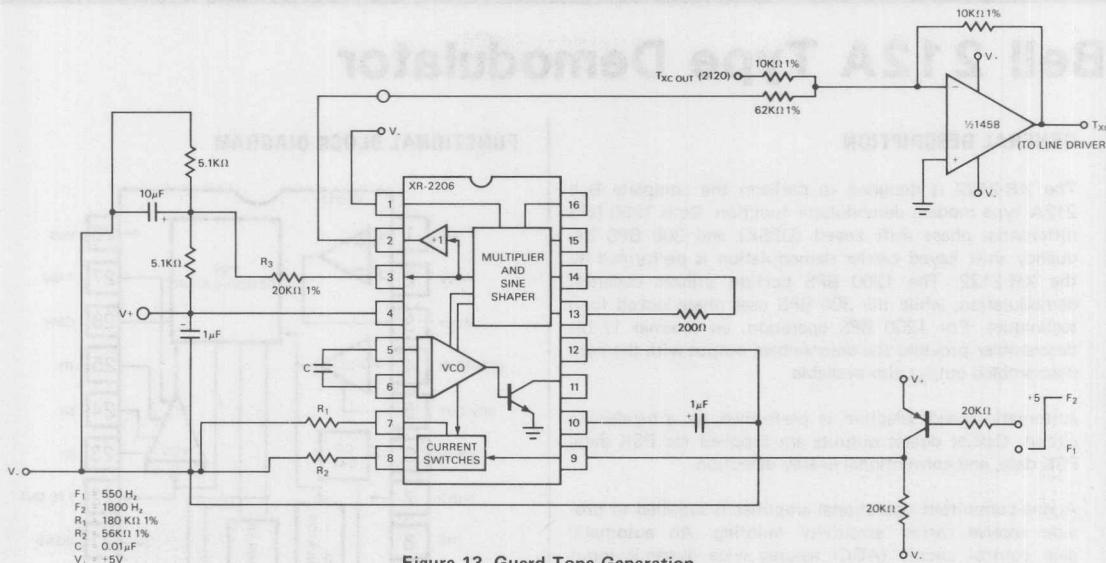
Figure 13. Guard Tone Generation

V.22 Guard Tone Generation

Figure 13 illustrates implementation of the V.22 guard tone generation. V.22 specifies use of the 1800 Hz guard tone in conjunction with the Originate carrier. The 550 Hz guard tone is a national option. Specifications for guard tone generation require the amplitude of the guard tone to be 6 ±1 dBM lower than' the transmitted carrier which is typically 9 dBM. The circuit of Figure 13 allows choice of implementation of either guard tone via TTL logic levels: 5 V giving 1800 Hz and 0 V producing 550 Hz. The 20 kΩ resistor to pin 3 sets the voltage at pin 2 to 1.2 V peak. This voltage is then summed and attenuated at the line driver (XR-1458) to give the -16 dBM output required.

Transmit Output Amplifier

To ensure transmit amplitude accuracy for the XR-2121, an external amplifier is recommended. The input to this amplifier should be from pin 3, T_{XC} ADJ. Figure 14 shows a typical implementation of this transmit amplifier.
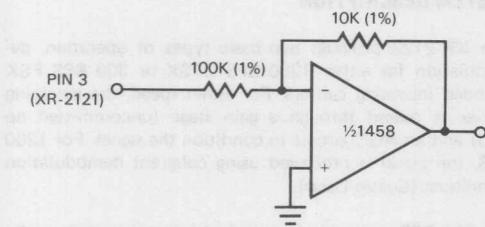
Figure 14. Transmit Carrier Output Amplifier

EXAR

Bell 212A Type Demodulator

GENERAL DESCRIPTION

The XR-2122 is designed to perform the complete Bell 212A type modem demodulator function. Both 1200 BPS differential phase shift keyed (DPSK) and 300 BPS frequency shift keyed carrier demodulation is performed by the XR-2122. The 1200 BPS portion utilizes coherent demodulation, while the 300 BPS uses phase-locked loop techniques. For 1200 BPS operation, an internal 17 bit descrambler provides the descrambled output with the non-descrambled output also available.

Automatic speed selection is performed by a handshake circuit. Carrier detect outputs are supplied for FSK data, PSK data, and conventional energy detection.

A non-committed operational amplifier is supplied to provide receive carrier sensitivity tailoring. An automatic gain control circuit (AGC) assures wide dynamic input carrier range.

The XR-2122 is constructed using silicon gate CMOS technology. The XR-2122 is designed to operate off of a 1.8432 MHz clock input. Available in a 28 Pin package, the XR-2122 is designed for +5 volt and -5 volt power supplies.

FEATURES

Bell 212A Compatible
1200 BPS DPSK Coherent Demodulation
300 BPS FSK Demodulation
Eye Diagram Output
Internal 17 Bit Descrambler
Non-descrambled Demodulation Output Available
FSK, PSK and Energy-type Carrier Detect Outputs
Automatic Speed Selection
Non-committed Op Amp for Input AGC Amplifier
AGC Input Circuit for Wide Dynamic Range

APPLICATIONS

Bell 212A Type Demodulator
Bell 103 Type Demodulator

ABSOLUTE MAXIMUM RATINGS

Power Supply
V_{DD} -0.3 to 7 V
V_{SS} 0.3 to -7 V
Input Voltage V_{SS} -0.3V to V_{DD} +0.3V
DC Input Voltage   ±10 mA
Power Dissipation   750 mW
   Derate Above 25°C   5 mW/°C
Storage Temperature Range   -65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM
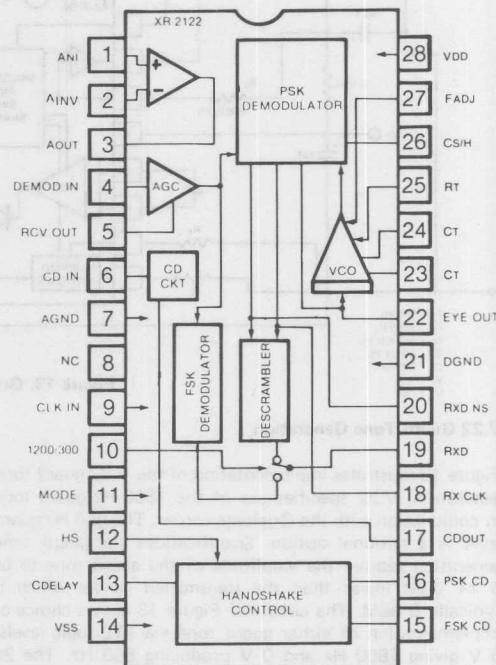
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2122CN	Ceramic	0°C to 70°C
XR-2122CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2122 provides two basic types of operation; demodulation for either 1200 BPS DPSK or 300 BPS FSK encoded incoming carriers. For either speed, the incoming carrier is passed through a gain stage (uncommitted op amp) and an AGC circuit to condition the signal. For 1200 BPS, the signal is processed using coherent demodulation techniques (Costas Loop).

For 300 BPS, a digital phase-locked loop type of demodulator is used providing low bias and jitter distortion without adjustments.

XR-2122

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V ± 5%, V_{SS} = -5 V ± 5%, T_A = 0-70°C, CLK IN = 1.8432 MHz ± .01%, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS						
I_{DD}	Quiescent Positive Supply Current		8	12	mA	Normal Operation
I_{SS}	Quiescent Negative Supply Current		-8	-12	mA	Normal Operation
DIGITAL CHARACTERISTICS						
I_{IN}	Input Current			10	μA	V_{IN} = V_{DD} or GND
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA
V_{OL}	Output Loss Voltage		0.4	0.8		I_{OL} = 2 mA
ANALOG CHARACTERISTICS (Circuit Configuration of Figure 11)						
A_{VG}	Amplifier Open Loop Gain		60		dB	
V_{DEMOD} IN	Typical Input Voltage to DEMOD IN		-6		dBm	
Z_{DEMOD} IN	DEMOD IN Input Impedance		15		KΩ	
$Z_{CD\ IN}$	CD IN Input Impedance		50		KΩ	
CD ON	CD On Level		-32	-30.5	dBm	T_A = 25°C
CD OFF	CD Off Level	-35.5	-34		dBm	T_A = 25°C
T_d CD	CD Off/On Delay Time	10	17	24	ms	
T_{dlh} FSK	FSK CD Off/On Delay Time	105	150	205	ms	
T_{dhl} FSK	FSK CD On/Off Delay Time	10	17	24	ms	
T_{dlh} PSK	PSK CD Off/On Delay Time	200	270	350	ms	C Delay = 0.47 μF
T_{dhl} PSK	PSK CD On/Off Delay Time	10	17	24	ms	
f_{VCO}	VCO Frequency Answer Mode Originate Mode		4.8 9.6		KHz Khz	

EQUIVALENT SCHEMATIC DIAGRAM
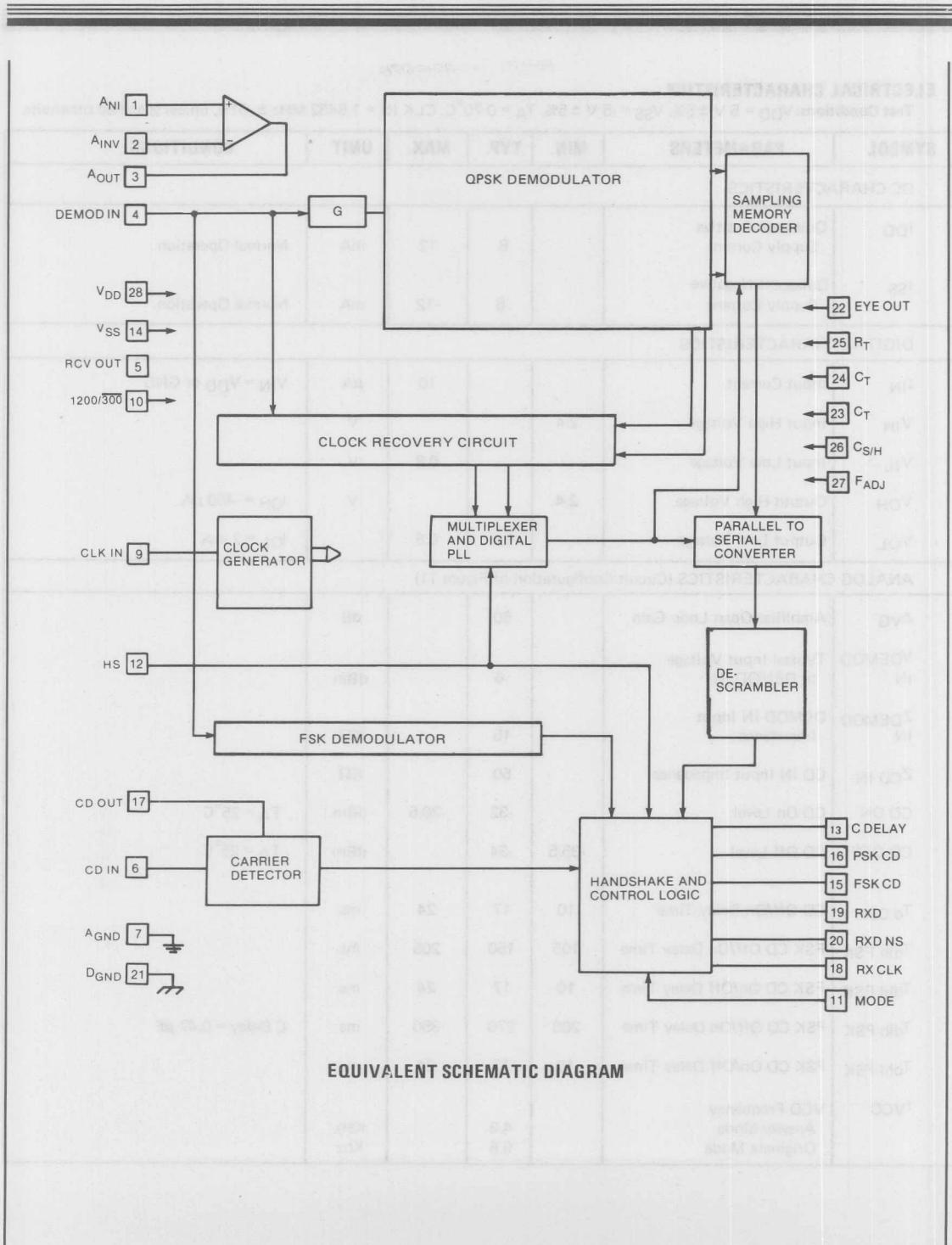
XR-2122

PRINCIPLES OF OPERATION

The XR-2122 is designed to perform the complete demodulator function in a Bell 212A type modem system. It has been specifically designed to complement the XR-2120 filter, XR-2121 modulator, and XR-2125 data buffer to form a four chip Bell 212A type modem signal processor. This four chip set is known as the XR-212AS and is covered in depth in Application Note AN-28. This data sheet will deal specifically with the XR-2122 and its functions.

The XR-2122 performs two different types of demodulation; 300 BPS frequency shift keyed (FSK) and 1200 BPS differential phase shift keyed (DPSK) encoded carriers.

First consider the 1200 BPS type of demodulation. For this demodulator operation, the XR-2122 accepts a DPSK encoded carrier (R_{XC}) typically from the telephone switched network, and demodulates it to produce a serial received data output. This serial data stream is synchronous, that is a clock, R_X $_{CLK}$, is used for synchronization purposes.

The DSPK encoded receive carrier, R_{XC}, is first applied to an automatic gain control circuit, AGC. This circuit, shown in Figure 1, provides a constant voltage output for a wide dynamic range input signal.
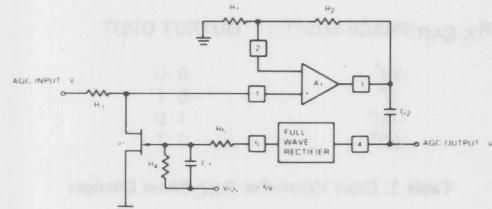
Figure 1. AGC Circuit

Operation of the AGC is as follows. V_O is internally set to about 1.5 volt peak-to-peak. The gain (non-inverting) of A_1 is set by R_2 and R_1, and is R_2/R_1 for $R_2 \gg R_1$. With the gain of A_1 set and a constant V_O, the input voltage to A_1's non-inverting input will be a constant voltage: $V_{NI} = (V_O) \div (R_2/R_1)$. FET Q_1 acts as a variable resistor to form a voltage divider with R_3 for the input signal. Q_1's resistance is controlled by the feedback path from A_1's output, through C_2, the full-wave rectifier and filter network R_4-R_5-C_1. The feedback will control the resistance of Q_1 in such a way that the voltage divider action it produces with R_3 will produce the precise voltage at V_{NI} of A_1, which, when multiplied by A_1's gain, will produce the correct V_O. Values are given in the applications section for a typical circuit which will accept an input dynamic range of -40 dBM to 0 dBM.

The output of the AGC, which is really a constant amplitude R_{XC}, is fed to two different circuits. One is for carrier recovery and one for clock recovery. The carrier recovery circuit is a Costas Loop. The error voltage outputs of the Costas Loop are fed to a sampling memory decoder which will produce dibits, or pairs of bits, which are extracted from each R_{XC} phase change. Figures A, B, and C show the eye diagram at the output of the Costas Loop with the receive clock, R_X $_{CLK}$. The eye diagram is the prime indicator of demodulation quality in a cohert type demodulator. The R_X $_{CLK}$ sets the point where the eye is sampled, which should be at the point of zero intersymbol interference, or, in other words, at the eye's maximum opening. The three photographs were taken at Pin 22, eye out, with a complete modem signal processor utilizing the XR-2121 modulator, XR-2120 filter, and XR-2125 data buffer. The eye opening, or quality of demodulation, changes with different line (telephone) quality. The three photos show the eye and R_X $_{CLK}$ for:

A) Back-to-back operation, or two modems directly tied together, A1 is originate and A2 is answer mode.
B) A 3002, C2 conditioned phone line. B1 is originate and B2 is answer mode.
C) A 3002 C0 unconditioned phone line. C1 is originate and C2 is answer mode.
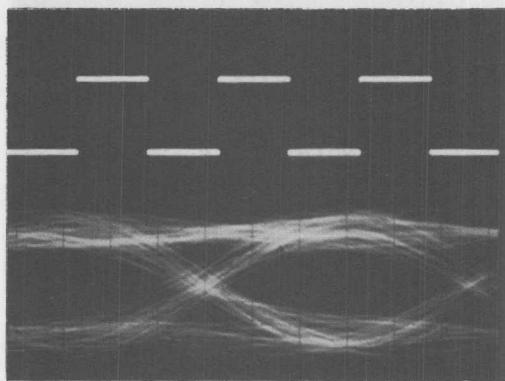
Figure. A1
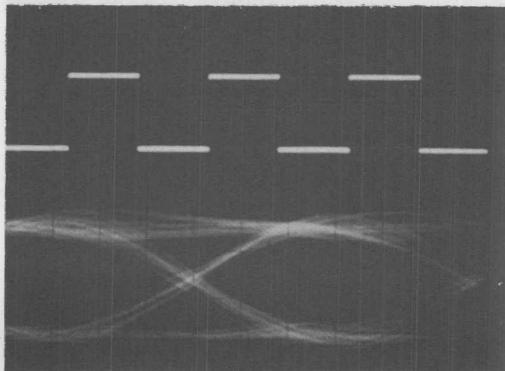
Figure. A2
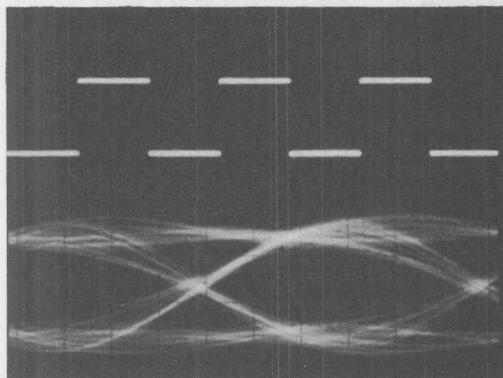
Figure. B1
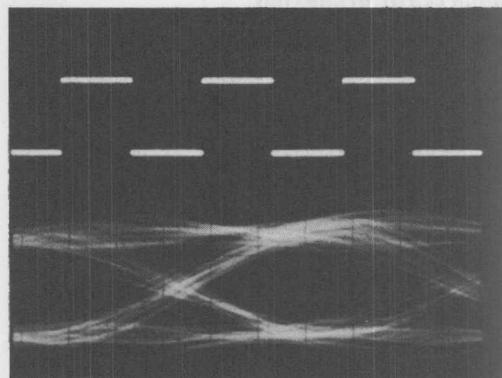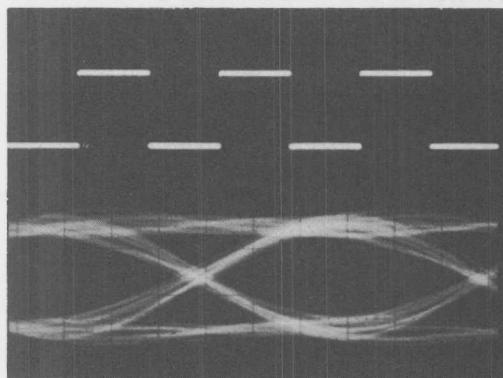
Figure. B2
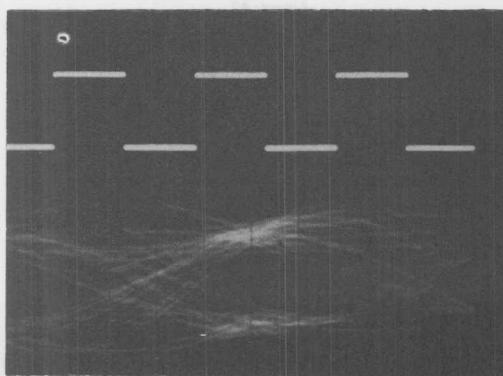
Figure. C1

Figure. C2

More information is given on this subject in Application Note AN-28. DPSK encoding introduces a phase shift to a constant frequency carrier every two data bits, or dibits (see XR-2121 modulator data sheet). Table 1 shows the four possible dibits for phase changes of R_{XC}. The XR-2122 conversely produces two data bits for each phase change. The two carrier frequencies are 1200 Hz and 2400 Hz; Table 2 shows the Mode/Frequency convention.

R_X CAR PHASE SHIFT	OUTPUT DIBIT
90°	0 0
0°	0 1
180°	1 0
-90°	1 1

Table 1. Dibit Values for R_{XC} Phase Changes

MODE	RECEIVE CARRIER FREQUENCY
Answer	1200 Hz
Originate	2400 Hz

Table 2. Carrier Frequency Assignments

The mode is controlled by a logic level on pin 10. The dibits are returned to serial form by a parallel to serial converter. Next, the serial data stream is descrambled; the circuitry for this function is shown in Figure 2.
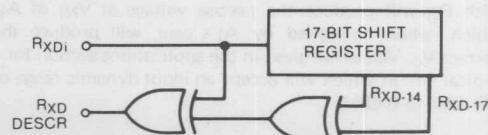
Figure 2. 17 Bit Psuedo Random Descrambler

The descrambler is necessary as all Bell 212A type modems use a scrambled data format for the 1200 BPS speed. This is used to insure that certain data patterns which would cause few, or no phase changes, ever exist. The output of the descrambler can be described by:

$$R_{XD} \text{ DESCR} = R_{XDI} (1 \oplus R_{XD}\text{-14} \oplus R_{XD}\text{-17})$$

For timing purposes during 1200 BPS operation, a clock must be extracted from the received carrier, R_{XC}. This clock represents a baud period and is 600 Hz. It is used internally for sampling and multiplied by two, 1200 Hz, and output on pin 18, R_X CLK. The timing relationship between R_X CLK and output data, R_{XD}, is shown in Figure 3.
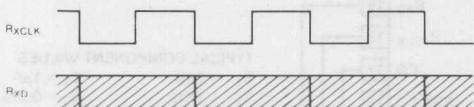
Figure 3. R_{XD}/R_X CLK Relationships

As seen in Figure 3, R_{XD} changes on the falling edge of R_X CLK.
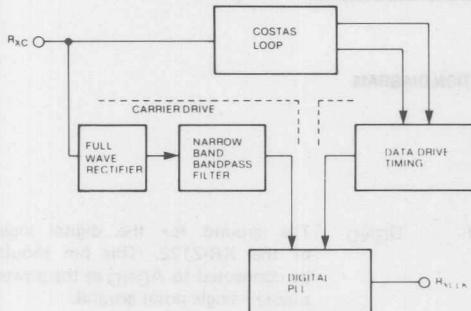
Figure 4. Timing Recovery Circuit

Clock recovery is accomplished from both the received carrier, R_{XC}, and data drive timing. Initially, the clock is recovered from R_{XC} for quick response and then assisted by the Costas Loop for data drive. A digital phase-locked loop, PLL, locks the two types of R_X CLK's together for a more stable clock. This clock is used internally for sampling and timing, and outputted on pin 18, R_X CLK, for sampling use externally.

The demodulation for the 300 BPS operation accepts an FSK encoded carrier and produces an asynchronous serial data output. Since it is asynchronous, no R_X CLK is used. The R_{XC} from the AGC output is fed to a digital phase-locked loop, PLL. The error voltage of the PLL is low pass filtered using switched capacitor filter techniques and compared against a reference voltage to produce the demodulated output.

The output of the two demodulators, FSK and DPSK, are fed into a handshake and control logic section. The primary purpose of this section is to decide whether the incoming carrier, RXC, is FSK or DPSK encoded, or, in other words, which speed the carrier modulation is: 300 BPS or 1200 BPS. This produces an auto speed control circuit. During the initial handshake routine, the XR-2122 will first look for an FSK R_{XC}. It does this by an FSK mark sensor which looks for five consecutive errors. If this condition occurs, operation will automatically be switched to 1200 BPS DPSK. The handshake circuit produces three carrier detect, CD, outputs; an FSK CD (pin 15), PSK CD (pin 16), and an energy level type CD (pin 17) which will respond to all in-band signals.

DESCRIPTION OF INPUTS AND OUTPUTS

Pin	Name	Description
1	A_{NI}	This is the input op amp non-inverting input. This op amp is typically used in the AGC circuit.
2	A_{INV}	The inverting input of the input op amp.
3	A_{OUT}	The output of the input op amp.
4	DEMOD	The input to both 300 BPS and 1200 BPS demodulators. Also the AGC output.
5	R_{CV} OUT	This pin is used to drive the gate of an external FET used in the AGC circuit.
6	CD IN	The input to the carrier detect circuitry.
7	AGND	Analog ground for the linear circuitry of the XR-2122. This ground should not carry logic current to avoid ground noise.
9	CLK IN	The master clock input, typically 1.8432 MHz ±0.01%.
10	$\overline{1200}/300$	Speed select input for selecting 1200 BPS DPSK or 300 BPS FSK operation.
11	MODE	Mode selection for answer or originate mode.
12	HS	Handshake enable/disable input. The handshake is primarily an auto speed selection circuit with a full description with the text section.
13	C_{DELAY}	Provides carrier detect turn-off and turn-on timing programming.
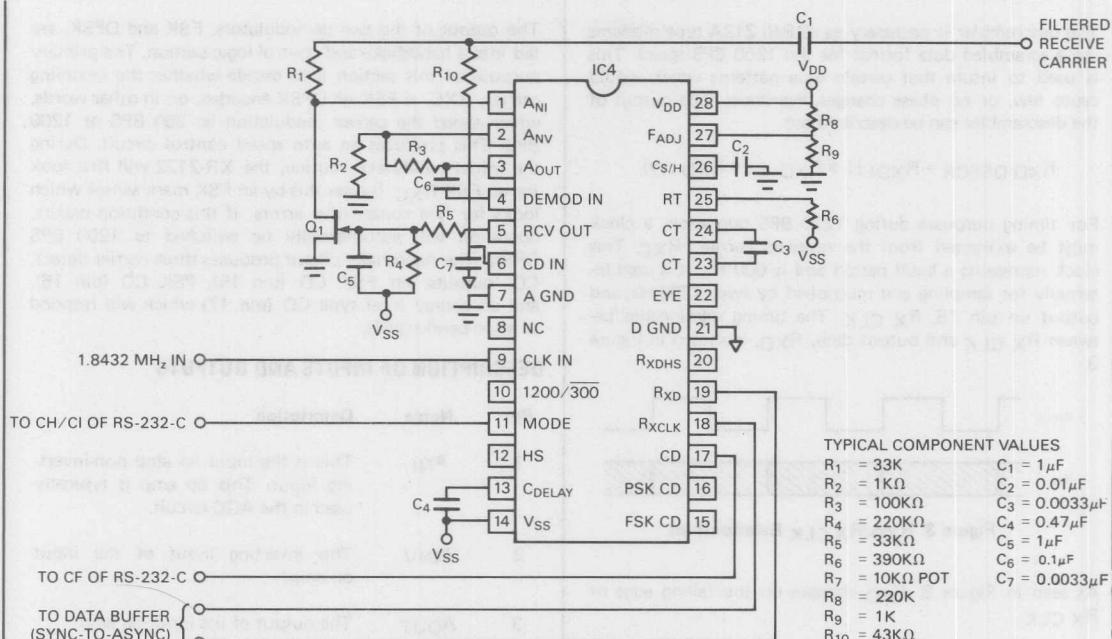
FIGURE 11. TYPICAL CONNECTION DIAGRAM

TYPICAL COMPONENT VALUES

R_1 = 33K	C_1 = 1μF
R_2 = 1KΩ	C_2 = 0.01μF
R_3 = 100KΩ	C_3 = 0.0033μF
R_4 = 220KΩ	C_4 = 0.47μF
R_5 = 33KΩ	C_5 = 1μF
R_6 = 390KΩ	C_6 = 0.1μF
R_7 = 10KΩ POT	C_7 = 0.0033μF
R_8 = 220K	
R_9 = 1K	
R_{10} = 43KΩ	

14	V_{SS}	Power supply input for the negative power supply. This supply is -5.0 ± 0.25 volts and should be well by-passed with decoupling capacitors.
15	FSK CD	This is the FSK CD output.
16	PSK CD	Provides the DPSK CD output.
17	CD	The energy-type CD output.
18	R_X CLK	Receive clock output which is a 1200 Hz square wave derived from the incoming DPSK encoded carrier, R_X CLK. Used for external timing of R_{XD}.
19	R_{XD}	Serial receive data output for either 1200 BPS DPSK or 300 BPS FSK.
20	R_{XD} NS	This provides a receive data output before the internal descrambler.

21	D_{GND}	The ground for the digital logic of the XR-2122. This pin should be connected to A_{GND} at the power supply - single point ground.
22	EYE	The Costas Loop eye diagram output is available at this pin.
23/24	C_T	The Costas Loop voltage controlled oscillator, VCO, timing capacitor is connected between these pins.
25	R_T	The Costas Loop VCO timing resistor.
26	$C_{S/H}$	Sample and hold capacitor is connected between this pin and analog ground, A_{GND}.
27	F_{ADJ}	Costas Loop VCO fine tuning input.
28	V_{DD}	Power supply input for the positive supply. This supply is +5.0 ± 0.25 volts and should be well bypassed with decoupling capacitors.

XR-2122

CONTROL INPUTS

Table 3 gives logic conditions for the various control inputs of the XR-2122.

| PIN | NAME | FUNCTION | |
		LOGIC HIGH	LOGIC LOW
10	1200/$\overline{300}$	1200 BPS DPSK Operation	300 BPS FSK Operation
11	MODE	Answer Originate	Originate
12	HS	Handshake Function/Enable	Handshake Function/Disabled

Table 3. Control Input Conditions

APPLICATIONS

The XR-2122 is shown in a typical connection in Figure 11.

In a complete modem system the received carrier, R_{XC}, would come from the receive filter such as the XR-2120. For the XR-2122 it would be either a FSK or DPSK encoded carrier typically from the telephone network. The data output, R_{XD}, would be either a 300 BPS serial bit asynchronous or 1200 BPS serial synchronous data stream. In a full application (AN-28), the R_{XD} output would go through the XR-2125 data buffer. For the 1200 BPS operation, the data buffer will convert the XR-2122 synchronous data into a character asynchronous format with a character length of 9 or 10 bits.

The input signal range of the R_{XC} is -40 dBM to 0 dBM for the AGC values given.

Figure 13 shows R8 and R9 replaced by potentiometer P_1.

Potentiometer P_1 adjusts an internal DC offset in the Costas Loop, or 1200 BPS section of the XR-2122. For optimum system performance, it should be adjusted for maximum eye opening at pin 22, EYE OUT (see Figure 12). Figure 13 shows the test set-up for observing the eye output of 1200 BPS and determining the demodulation quality.

MAXIMUM EYE OPENING
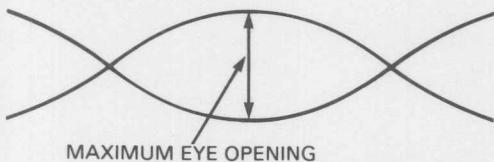
Figure 12. Eye Diagram Characteristics

Further, more complete applications information on the XR-2122 is given in Application Note AN-28 which covers the device used in a complete system.

Bell 212A Handshake Protocol

The XR-2122 performs the sensing for the Bell 212A handshake protocol. With the handshake pin, pin 12, pulled high (+5 V), the XR-2122 will perform energy and sensing and indication, and auto speed adjust. These functions can be utilized to complete the Bell 212A handshake. Timing parameters are illustrated in Figure 14A and 14B.

Since the XR-2122 will change speeds internally, overriding the speed selection pin (pin 10), the designer must provide a means for selecting the required handshake protocol carrier from the modulator, the XR-2121. This selection can be achieved in hardware or software.

Addendum:

Handshake:

The handshake pin (HS), pin 12, must be low when the device is first powered up. The reason for this is that at power up, the digital portions of the XR-2122 will reset to an initial state. The HS pin being high will prevent this from occurring. It is best to have the HS pin low for 2 seconds to allow the reset to completely finish.

AGC:

The requirements for the AGC Field Effect Transistor that is tied to pin 1 (A_{NI}) is as follows:

V_{GS} (gate-source cut-off voltage) =
      -0.8 V minimum, -4.0 V maximum
$V_{DS(on)}$ (drain-source on voltage =
      0.5 V at I_D = 5 mA maximum
$r_{ds(on)}$ (drain-source on resistance) =
      60 ohms maximum
BV_{GSS} (gate-source breakdown voltage =
      -30 V minimum

The 2N4681 meets these requirements and is used for all demonstrations in EXAR's labs.
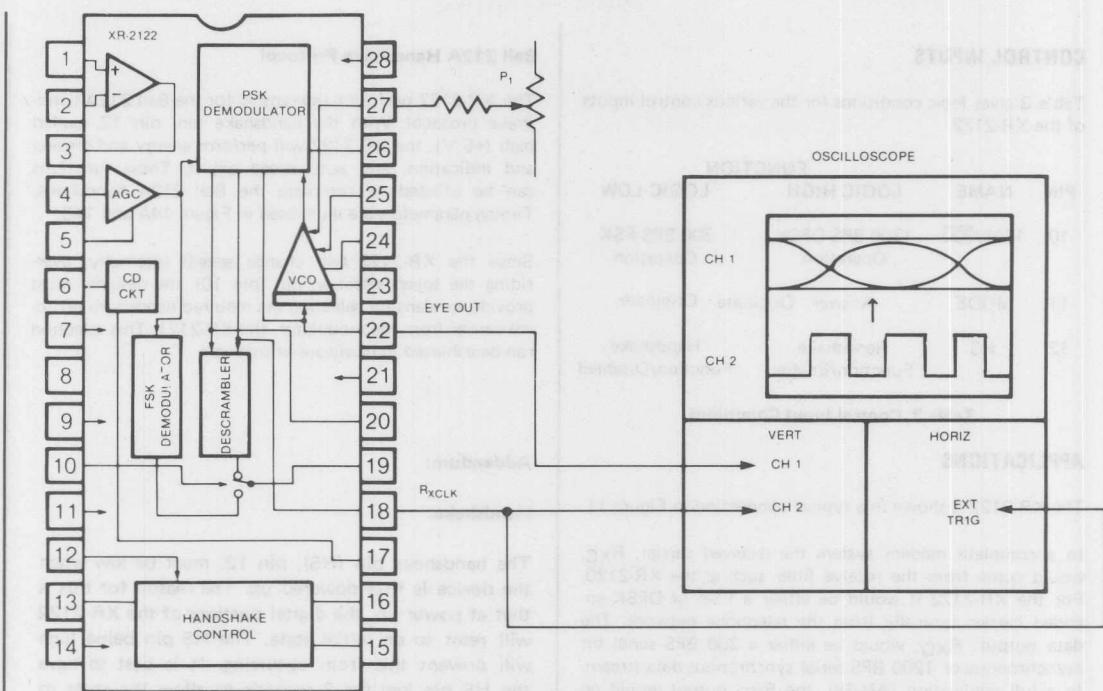
Figure 13. Set-up for Eye Diagram Output

ORIGINATING STATION

RECEIVE CARRIER |←——ANSWER TONE——→|

TRANSMIT CARRIER   1270 Hz

FSK CD

PSK CD   0.15 S

ANSWERING STATION

RECEIVE CARRIER   DATA

TRANSMIT CARRIER   DATA

FSK CD

PSK CD |←——— 0.890 S ———→| |←0.33 S→| 0.15 S
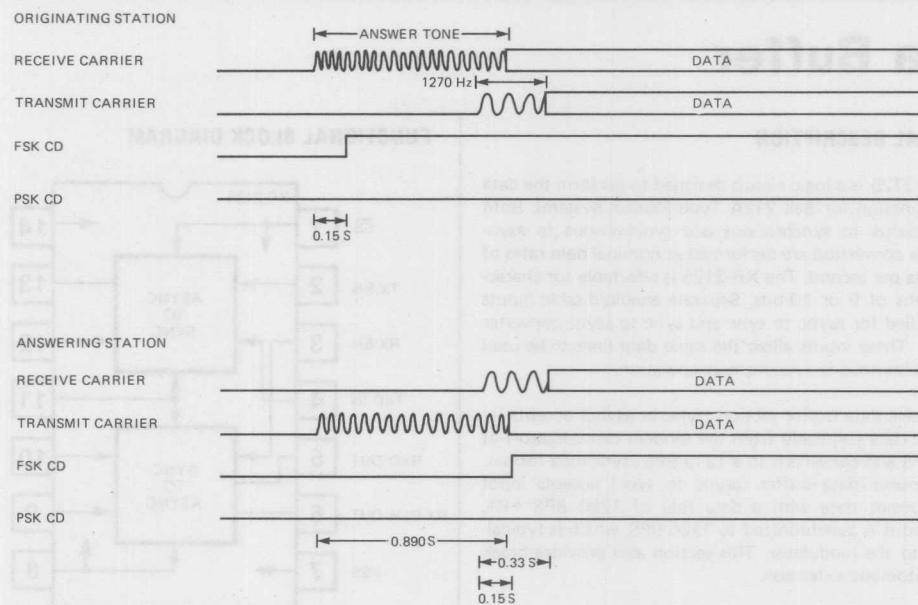
Figure 14A. 212A Handshake 300 BPS

ORIGINATING STATION

RECEIVE CARRIER |←——ANSWER TONE——→|←—2400 Hz MARK—→| DATA

TRANSMIT CARRIER |←——1200 Hz MARK——→| DATA

FSK CD

PSK CD   0.15 S   0.27 S

ANSWERING STATION

RECEIVE CARRIER |←———1200 Hz MARK———→| DATA

TRANSMIT CARRIER BILLING DELAY |←—ANSWER TONE—→|←—2400 Hz MARK—→| DATA

FSK CD

PSK CD   2 S   1 S   0.774 S   1.32 S   0.275

*Denotes scrambled
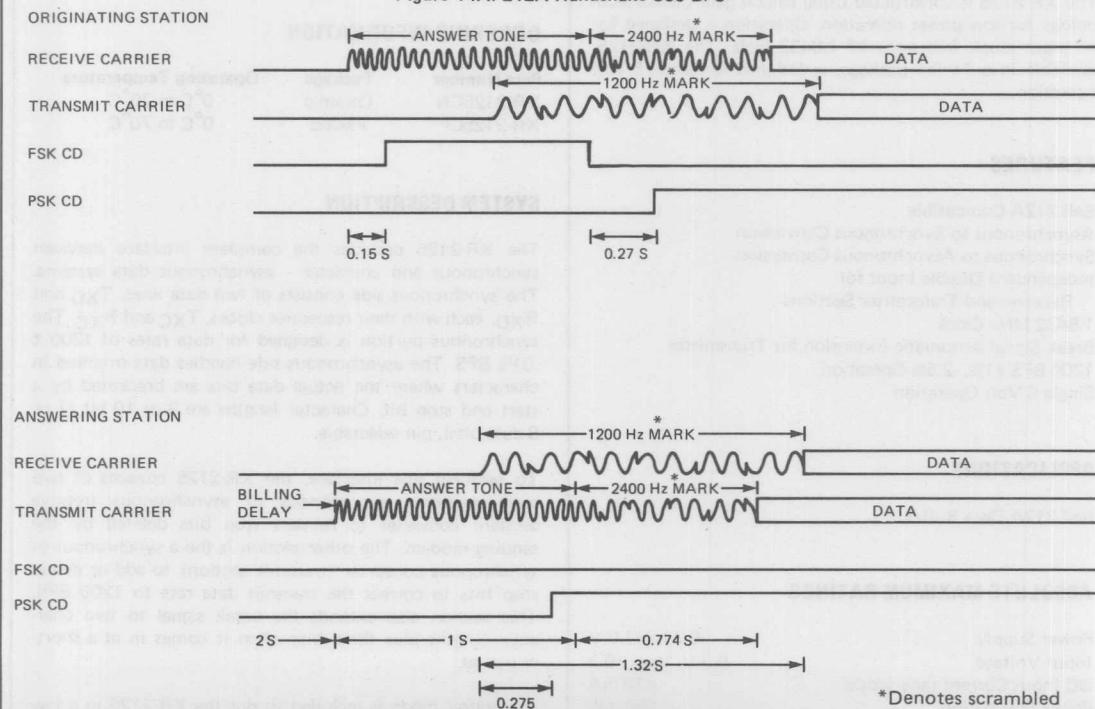
Figure 14B. 212A Handshake 1200 BPS

Data Buffer

GENERAL DESCRIPTION

The XR-2125 is a logic circuit designed to perform the data buffer function for Bell 212A Type Modem Systems. Both asynchronous to synchronous and synchronous to asynchronous conversion are performed at nominal data rates of 1200 bits per second. The XR-2125 is selectable for character lengths of 9 or 10 bits. Separate enable/disable inputs are supplied for async to sync and sync to async converter sections. These inputs allow the same data lines to be used for asynchronous or synchronous operation.

The receive data buffer section (sync to async) accepts input sync data (typically from the modem demodulator) at 1200 BPS and converts it to a 1219 BPS async data format. The transmit data buffer (async to sync) accepts input async format data with a data rate of 1200 BPS +1%, -2.5% and it is synchronized to 1200 BPS, which is typically sent to the modulator. This section also provides break signal automatic extension.

The XR-2125 is constructed using silicon gate CMOS technology for low power operation. Operation is designed for an input clock frequency of 1.8432 mHz. The XR-2125, available in a 14 Pin package, is designed for single 5 volt operation.

FEATURES

Bell 212A Compatible
Asynchronous to Synchronous Conversion
Synchronous to Asynchronous Conversion
Independent Disable Input for
  Receiver and Transmitter Sections
1.8432 MHz Clock
Break Signal Automatic Extension for Transmitter
1200 BPS +1%, -2.5% Operation
Single 5 Volt Operation

APPLICATIONS

Bell 212A Data Buffer

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3 to +7.0 V
Input Voltage	-0.3 to V_{DD} +0.3
DC Input Current (any input)	±10 mA
Power Dissipation	250 mW
Storage Temperature Range	-65°C to +125°C

FUNCTIONAL BLOCK DIAGRAM
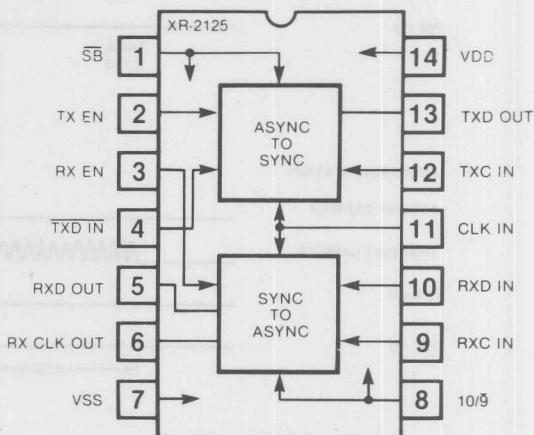
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2125CN	Ceramic	0°C to 70°C
XR-2125CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2125 provides the complete interface between synchronous and character - asynchronous data systems. The synchronous side consists of two data lines, T_{XD} and R_{XD}, each with their respective clocks, T_{XC} and R_{XC}. The synchronous portion is designed for data rates of 1200 ± .01% BPS. The asynchronous side handles data oriented in characters where the actual data bits are bracketed by a start and stop bit. Character lengths are 9 or 10 bit (7 or 8 data bits), pin selectable.

To perform this interface, the XR-2125 consists of two main sections: synchronous to asynchronous (receive section) converter to reinsert stop bits deleted by the sending modem. The other section is the a synchronous to synchronous converter (transmit section) to add or delete stop bits to correct the transmit data rate to 1200 BPS. This section also extends the break signal to two character lengths plus three bits when it comes in at a shorter period.

A standby mode is included to put the XR-2125 in a low supply current, non-operative, mode on command.

XR-2125

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V ± 5%, T_A = 0-70°C, CLK IN = 1.8432 MHz ±0.01%, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS						
V_{OL}	Output Low Voltage		0.05	0.8	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OM} = −400 μA
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
I_{OL}	Output Low Current		2		mA	
I_{OH}	Output High Current			−400	μA	
I_{IN}	Input Current			±10	μA	V_{IN} = 0 - V_{DD}
I_{DD}	Supply Current Quiesent		100	250	μA	
I_{DD}	Supply Current Standby			10	μA	
AC CHARACTERISTICS: $f_{TXC\ IN}$ = 1200 ±0.01% Hz, $f_{RXC\ IN}$ = 1200 ±0.01% Hz.						
t_{wstr}	Start Bit Width		820		μs	
t_{wstp}	Stop Bit Width 9 Bit Character 10 Bit Character		 938 951		 μs μs	Reinserted Stop Bits and (n) (820 μs) long
f_{txd}	TXD in Bit Rate	1170	1200	1212	BPS	
t_{dtxd}	TXD Out Delay Time			200	ns	C_L = 50 pf; $10/\overline{9}$ = Hi
t_{drxd}	RXD Out Delay Time			200	ns	$10/\overline{9}$ = Hi
f_{rxco}	RXC Out Frequency		1219		Hz	
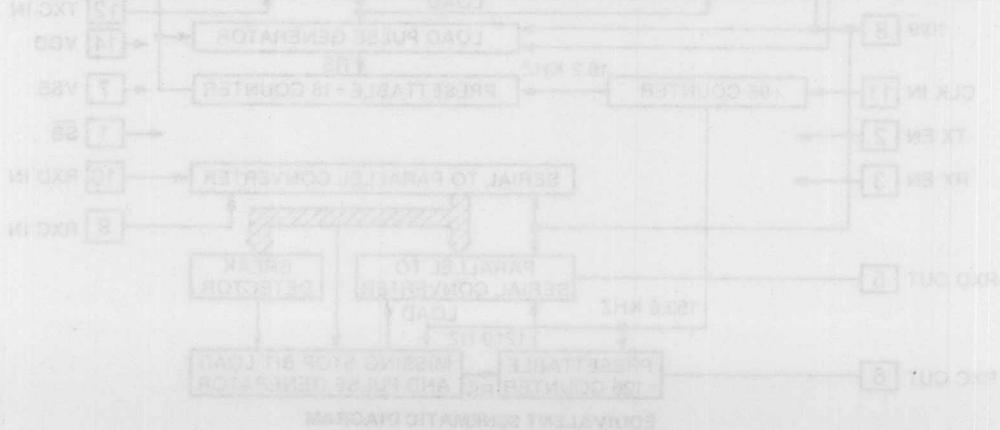
RECEIVE TIMING
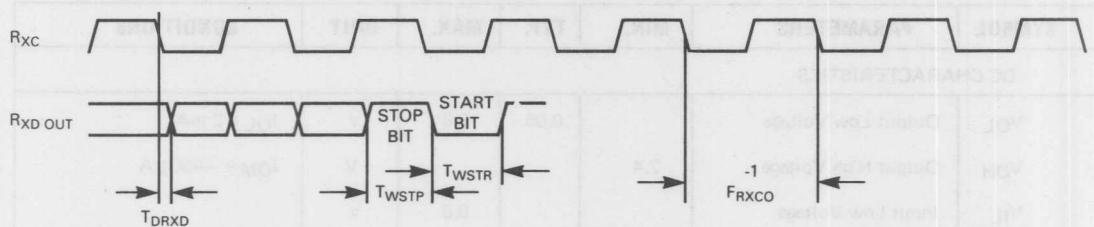
TRANSMIT TIMING
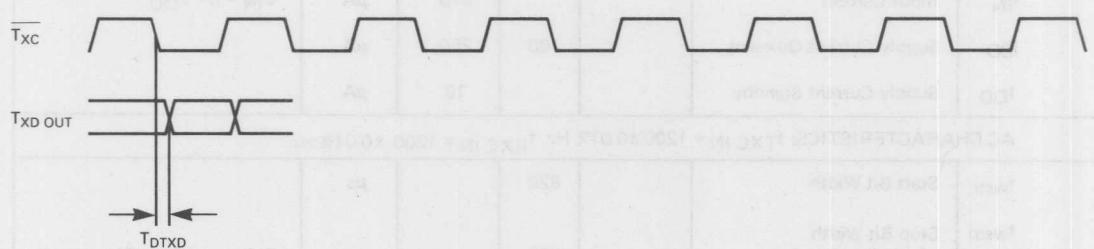
TRANSMIT AND RECEIVE TIMING CHARACTERISTICS
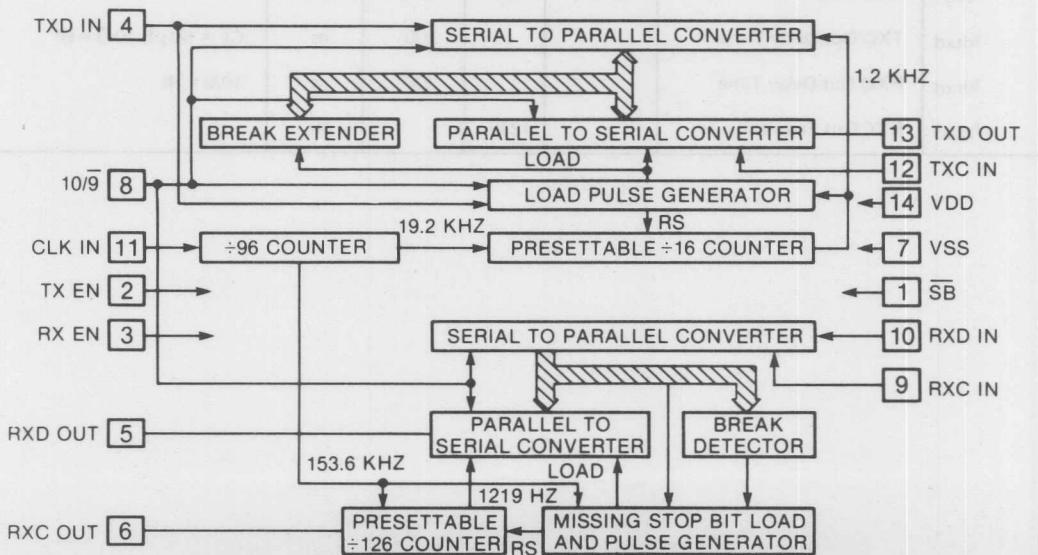
EQUIVALENT SCHEMATIC DIAGRAM

XR-2125

DESCRIPTION OF INPUTS AND OUTPUTS

| Pin	Name	Description
1	$\overline{SB}$	This pin places the XR-2125 in a non-operative, low quiescent current mode.
2	T_{XEN}	An enable input for the transmitter section (async to sync). When enabled, async to sync conversion is performed on $T_{XD\ IN}$. When disabled, the data on $T_{XD\ OUT}$ will be identical to that of $T_{XD\ IN}$ (flow through mode) In Bell 212A type modem applications the sync to async will be disabled for 300 BPS FSK operation and for 1200 BPS synchronous operation.
3	$R_X\ EN$	An enable input for the receiver section (sync to async). When enabled, sync to async conversion is performed on $R_{XD\ IN}$. When disabled, the data on $R_{X\ OUT}$ will be identical to that of $R_{XD\ IN}$ (flow through mode). In Bell 212A type modem applications the sync to async will be disabled for 300 BPS FSK operation and for 1200 BPS synchronous operation.
4	$T_{XD\ IN}$	The transmitter data input. This is a serial data stream with a data rate of 1200 BPS +1%/-2.5% ($T_X\ EN$ active).
5	$R_{XD\ OUT}$	The asynchronous serial data out from the sync to async converter ($R_X\ EN$ active). The data rate of this signal is 1219 BPS.
6	$R_X\ CLK\ OUT$	Received clock output.
7	V_{SS}	Ground pin.
8	$10/\overline{9}$	Asynchronous character length selection input. Ten bit (start bit, 8 data bits and a stop bit) or nine bit (7 data bits) can be selected.
9	$R_{XC\ IN}$	The receive clock input, which typically is supplied by the demodulator (XR-2122). The frequency should be 1200 Hz ± 0.01%.
10	$R_{XD\ IN}$	The synchronous serial data input which is typicall from the demodulator data output (R_{XD} of the XR-2122). The data rate of this signal is 1200 BPS ± 0.01%.
11	CLK IN	Master clock input of 1.8432 Hz ± 0.01%.
12	$T_{XC\ IN}$	The transmit clock input which is typically supplied by the modulator (XR-2121). The frequency should be 1200 Hz ± 0.01%.
13	$T_{XD\ OUT}$	The synchronous serial data output which typically goes to the modulator input (XR-2121). The data rate of this signal is 1200 BPS ± 0.01%.
14	V_{DD}	This pin provides the input for the positive power supply which should be +5 ± 0.25 volts.

CONTROL INPUTS

Table 1 gives the logic conditions for the various control inputs of the XR-2125.

		FUNCTION	
PIN	NAME	LOGIC HIGH	LOGIC LOW
1	$\overline{SB}$	Normal Operation	Standby Mode
2	T_{XEN}	Transmitter Enabled	Transmitter Disabled
3	R_{XEN}	Receiver Enabled	Receiver Disabled
8	$10/\overline{9}$	10 Bit Character	9 Bit Character

Table 1. Control Input Conditions

PRINCIPLES OF OPERATION

The XR-2125 performs the complete asynchronous to synchronous and synchronous to asynchronous conversion on the serial transmit and receive data paths in a Bell 212A type modem. This conversion allows the synch modulator/demodulator such as the XR-2121/XR-2122 to communicate with the async DTE. The async format is character type as shown in Figure 1.
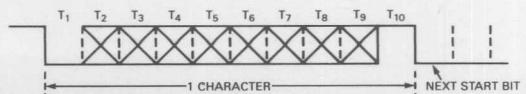
Figure 1. Async Character

Figure 1 shows each character starting with a start bit (T1) followed by either 7 or 8 data bits (8 shown → T2 - T9) and ending by a stop bit T10) this makes a total character length of either 9 or 10 bits, which the XR-2125 can be selected for by pin 8, 10/9.

The XR-2125 can also provide "flow through" operation by disabling the transmit and receive sections using pins 2 and 3, T_{XEN} and R_{XEN}. This mode would be used for 1200 BPS sync mode or 300 BPS bit async operation.

Figure 2 illustrates a typical connection of the XR-2125. Pins 2 and 3 (T_{XEN} and R_{XEN}) are used to toggle the

XR-2125 into the high speed asynchronous mode. The main function of the XR-2125 is to synchronize asyn-- chronous data (1200 BPS + 1% - 2.5%) from the DTE to synchronous data (1200 BPS) for the modulator, and to take synchronous demodulated data (1200 BPS) and conver it to the 1219 BPS asynchronous format for the DTE.

The break detector serves to distinguish between an actual break character and two consecutive nulls with the stop bit deleted. It forces reinsertion of the stop bit between the nulls and passes

Pin				Pin	
1	$\overline{SB}$		V_{DD}	14	
HIGH SPEED ASYNCHRONOUS SELECT ○——	2	T_X EN	T_{XD} OUT	13	——○ TO MODULATOR $T_{XC\ IN}$
	3	R_X EN	T_{XC} IN	12	——○ FROM MODULATOR T_{XCLK}
TRANSMIT DATA FROM DTE ○——	4	T_{XD} IN	CLK IN	11	——○ 1.8432 MHz INPUT
RECEIVED DATA TO DTE ○——	5	R_{XD} OUT	R_{XD} IN	10	——○ FROM DEMODULATOR $R_{XD\ OUT}$
	6	R_X CLK OUT	R_{XC} IN	9	——○ FROM DEMODULATOR R_{XCLK}
	7	V_{SS}	10/9	8	——○ CHARACTER LENGTH SELECT
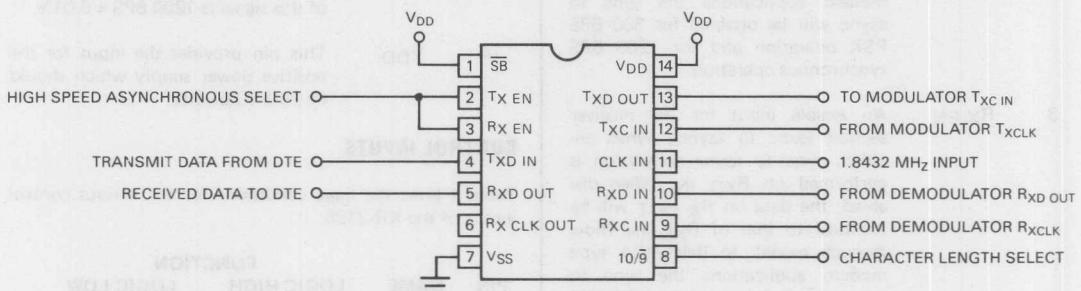
Figure 2. Typical Connection XR-2125

EXAR

Bell 212A/CCITT V.22 Modem Filters

GENERAL DESCRIPTION

The XR-2126/2127/2128/2129 modem filters are monolithic CMOS switched capacitor filters designed for use in full duplex 1200 BPS modems. They meet all the filtering functions of the Bell 212A and CCITT V.22 modem specifications. They include the low band (centered at 1200 Hz) and high band (centered at 2400 Hz) filters with full channel compromise equalization and output smoothing filters for both bands.

For CCITT V.22 applications, a notch filter is included that can be selected for either 550 Hz or 1800 Hz and provide greater than 55 dB of rejection at these frequencies. Also included in these devices are two uncommitted operational amplifiers which can be used for input anti-aliasing filtering or for additional gain, and additional equalization for Worst Case Line (3002, C_O) conditions.

The XR-2126 is pin and function compatible to the AMI S35212 while the XR-2127 is pin and function compatible to the AMI S35212A. The XR-2128 is an enchanced version of the XR-2126 and XR-2127. Like the S35212 and S35212A, the high band filter in the XR-2126, XR-2127 and XR-2128 can be scaled down by a factor of 6 so it can be used to monitor Call Progress tones in smart modems. And, like the S35212A, the XR-2127 and XR-2128 have analog loop back mode for testing the functions of the modem.

The XR-2128 contains two additional control pins, CPM (Pin 12) and NFI (Pin 13), that allow more accurate Call Progress Monitoring and easier V.22 implementation without the need for external multiplexers and smoothing filters. The CPM pin scales the low band filter by a factor of 2.5 for better centering over the Call Progress frequency range of 300 to 660 Hz, allowing the unscaled high band filter to be used for monitoring the modem answer tone.

The XR-2129 is an EXAR version of the 212A/V.22 modem filter. All the features of the XR-2126/2127/2128 except the clock frequencies are provided. The XR-2129 operates from a 1.8432 MHz crystal with an onboard clock oscillator. It also features a 1.8432 MHz buffered clock output and 10 dB of gain in the receive path. When used with the XR-2121 modulator, XR-2122 demodulator, and XR-2125 buffer, and a small amount of external circuitry, all the functions needed to realize the Bell 212A modem are in place.

APPLICATIONS

Bell 212A Modem Filtering
CCITT V.22 / V.22bis Modem Filtering
Bell 103 Modem Filtering
Other Modem Filter Applications

FUNCTIONAL BLOCK DIAGRAMS
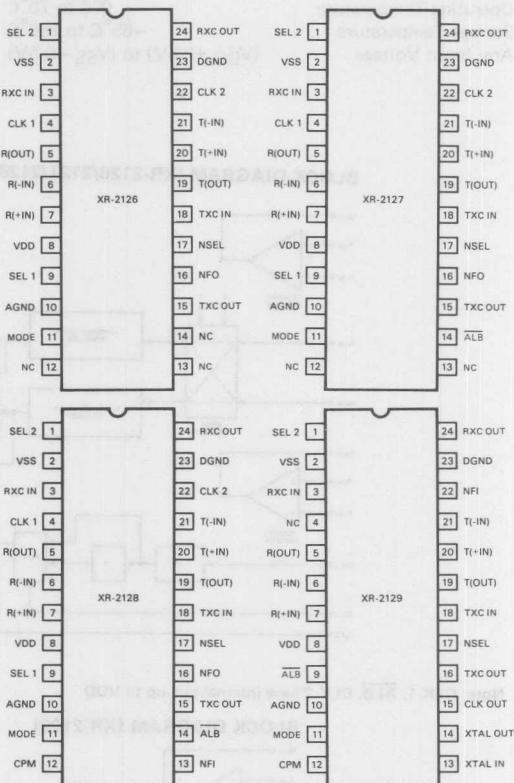
FEATURES

Bell 212A/CCITT V.22 Compatible Transmit and Receive
   Filters with Full Channel Compromise Equalization
Selectable V.22 Notch Filters Included (550 Hz/1800 Hz)
Built-in Call Progress Mode/Enhanced Call Progress Mode
Analog Loop Back Capability
Phone Line Status Monitor Capability (Bypass Mode)
Additional Equilization for Worst Case Line
   (3002, C_O) Conditions (XR-2128/XR-2129 only)
On-chip Transmit and Receive Output Smoothing Filters
Two Uncommitted Operational Amplifiers
Choice of Clock Frequencies:
   153.6 KHz or 1.2288 MHz/2.4576 MHz on XR-2126,
   XR-2127, XR-2128
   1.8432 MHz Crystal with On-Chip Clock Oscillator
   on XR-2129
TTL/CMOS Compatible Digital Inputs

XR-2126/7/8/9

ABSOLUTE MAXIMUM RATINGS

Power Supply	12V (±6V)
Power Dissipation, Plastic	1.0W
Derate Above 25°C	5 mW/°C
Power Dissipation, Ceramic	1.3W
Derate Above 25°C	7 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to 150°C
Any Input Voltage	$(V_{DD} +0.5V)$ to $(V_{SS} -0.5V)$

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2126CN	Ceramic	0°C to 70°C
XR-2126CP	Plastic	0°C to 70°C
XR-2127CN	Ceramic	0°C to 70°C
XR-2127CP	Plastic	0°C to 70°C
XR-2128CN	Ceramic	0°C to 70°C
XR-2128CP	Plastic	0°C to 70°C
XR-2129CN	Ceramic	0°C to 70°C
XR-2129CP	Plastic	0°C to 70°C

All devices are also available in Surface Mount Packages. Consult factory for complete information.

BLOCK DIAGRAM (XR-2126/2127/2128)

Note: CLK 1, ALB, CLK 2 have internal pull-up to VDD
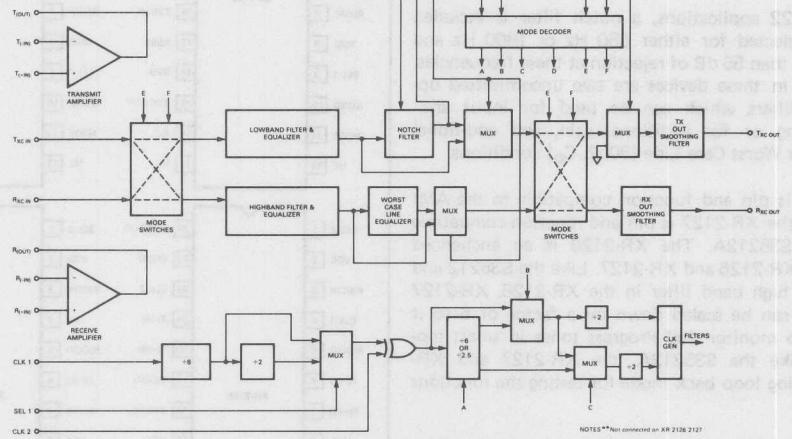
NOTES ** Not connected on XR 2126 2127
* Not connected on XR 2126

Note: SEL 2, SEL 1, MODE, CPM, NFI have internal pull-down to ground

BLOCK DIAGRAM (XR-2129)
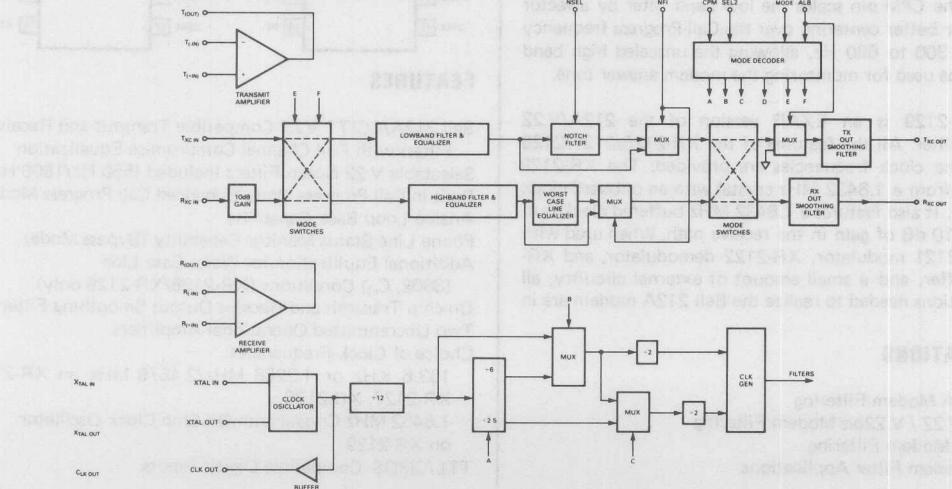
DC ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 0°C$ to $70°C$, $V_{DD} = +5V$ ±5%, $V_{SS} = -5V$ ±5%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{DD}	Quiescent Current		15		mA	
I_{SS}	Quiescent Current		15		mA	
V_{IH}	High Level Input Voltage, Digital Signal Pins		2.5		V	Note 1
V_{IL}	Low Level Input Voltage, Digital Signal Pins		0.8		V	Note 2
V_{OH}	High Level Output Voltage	2.6			V	
V_{OL}	Low Level Output Voltage			0.5	V	

AC ELECTRICAL CHARACTERISTICS

Test Conditions: $25°C$, $V_{DD} = +5V$, $V_{SS} = -5V$, unless specified otherwise.

| SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
f_c	Low Band Center Frequency	1190	1200	1210	Hz	
	High Band Center Frequency	2380	2400	2420	Hz	
	Adjacent Channel Rejection					
	Low Band	55	65		dB	
	High Band	55	75		dB	
f_{BW}	3 dB Bandwidth		950		Hz	
	Pass Band Gain at Center Frequency	−.5		+.5	dB	1200 Hz, 2400 Hz
	Crosstalk		65		dB	
	Dynamic Range		70		dB	
THD	Total Harmonic Distortion		0.3		%	
E_n	Output Noise		1	2	mVrms	In Passband
	Stop Band Rejection					
	Low Band Filter		30		dB	At 500 Hz
			25		dB	At 1800 Hz
			75		dB	At 2400 Hz
			43		dB	At 4000 Hz
	High Band Filter		55		dB	At 500 Hz
			95		dB	At 1200 Hz
			25		dB	At 1800 Hz
			35		dB	At 4000 Hz
	NFI = High		65		dB	At 550 Hz, NSEL = Low
			65		dB	At 1800 Hz, NSEL = High
	Group Delay					
	Low Band Filter		5160		μsec	At 900 Hz
			5300		μsec	At 1200 Hz
			5360		μsec	At 1500 Hz
	High Band Filter		5370		μsec	At 2100 Hz
			5110		μsec	At 2400 Hz
			4900		μsec	At 2700 Hz
	Output Voltage Swing		8.0		Vp-p	

Note 1: $V_{in} > V_{IH}$ is a logic 1.
Note 2: $V_{in} < V_{IL}$ is a logic 0.

XR-2126/7/8/9

The following table lists EXAR filters and their pin compatible counterparts.

EXAR	Counterpart	
XR-2126	AMI	S35212
	Reticon	RM5632A
XR-2127	AMI	S35212A
	Sierra	SC11005
XR-2128	Sierra	SC11001
XR-2129	none	

PIN DESCRIPTIONS

Pin	Name	Desciption/Function
1	SEL 2	Call Progress mode selection; SEL 2 logic 0 for normal operation, SEL 2 logic 1 scales down the high band filter by 6 for Call Progress Monitoring.
2	VSS	Negative supply voltage (typically −5V). A decoupling capacitor of 0.1µF to ground is required.
3	RXC IN	Receive signal input.
4	CLK 1	Clock input 1 on XR-2126/2127/2128; 2.4576 MHz with SEL 1 logic 1 or 1.2288 MHz with SEL 1 logic 0, TTL or CMOS compatible.
	NC	No connection on XR-2129.
5	R(OUT)	Receive uncommitted operational amplifier output.
6	R(−IN)	Inverting input of the receive uncommitted operation amplifier.
7	R(+IN)	Non-inverting input of the receive uncommitted operational amplifier.
8	VDD	Positive supply voltage (typically +5V). A decoupling capacitor of 0.1µF to ground is required.
9	SEL 1	Selects clock frequency into Pin 4 on XR-2126/2127/2128; logic 0 for 1.2288 MHz, logic 1 for 2.4576 MHz.
	ALB	Analog loop back on XR-2129; logic 1 for normal operation, logic 0 to internally loop back TXC OUT to RXC OUT with no signal (MUTE) on TXC OUT.
10	AGND	Analog ground.
11	MODE	Originate/Answer mode selection; logic 0 for Originate, logic 1 for Answer.
12	NC	No connection on XR-2126/2127.
	CPM	Enhanced Call Progress Mode selection on XR-2128 and XR-2129; CPM logic 0 for normal operation; CPM logic 1 scales down the low band filter by 2.5 for enhanced Call Progress Monitoring.
13	NC	No connection on XR-2126/2127.
	NFI	Notch filter insert pin on XR-2128; logic 0 for notch filter bypass (Bell 212A), logic 1 for inserting 550 Hz/ 1800 Hz notch (V.22).
	XTAL IN	XR-2129 only. On chip oscillator for input requiring 1.8432 MHz crystal connected across XTAL OUT and XTAL IN. No external resistors or capacitors are required.
14	NC	No connection on XR-2126.
	ALB	Analog loop back on XR-2127 and XR-2128. Same as Pin 9 on XR-2129.
	XTAL OUT	XR-2129 only. Unbuffered oscillator output.
15	TXC OUT	Transmit output signal on XR-2126, XR-2127, XR-2128. With a 2.2kΩ pull down resistor to VSS this output will drive 1500Ω typically.
	CLK OUT	1.8432 MHz buffered clock output on XR-2129.
16	NFO	Buffered notch filter output on XR-2126, XR-2127, XR-2128
	TXC OUT	Transmit output signal on XR-2129. Same as Pin 15 on XR-2126/2127/ 2128.
17	NSEL	Notch filter selection; logic 0 for 550 Hz, logic 1 for 1800 Hz.
18	TXC IN	Transmit input signal.
19	T(OUT)	Transmit uncommitted operational amplifier output.
20	T(+IN)	Non-inverting input of the transmit uncommitted operation amplifier.
21	T(−IN)	Inverting input of the transmit uncommitted operational amplifier.

22	CLK 2	Clock input 2 on XR-2126/2127/2128. 153.6 KHz TTL or CMOS clock.
	NFI	Notch filter insert pin on XR-2129, same as Pin 13 on XR-2128.
23	DGND	Digital ground.
24	RXC OUT	Receive output signal.

PRINCIPLES OF OPERATION

Low Band Filter

The low band filter is a 20th order switched capacitor filter consisting of a 10th order bandpass filter centered at 1200 Hz and a 10th order allpass filter centered at 1200 Hz. The allpass filter is a delay equalizer that provides compensation for the pass band group delay variation in the low band filter and half of the compromise line characteristics. See Figure 1 for the group delay response and Figure 2 for amplitude response.

In the Originate mode, the low band is used in the transmit path and in the Answer mode, it is used in the receive path. When analog loop back is used in the Originate mode, the low band filter will be in the test loop. In Call Progress Monitoring mode with SEL 2 (Pin 1) at logic 1, and CPM (Pin 12) at logic 0, the center frequency of the filter will be shifted down by a factor of 6 to 250 Hz. If CPM (Pin 12) is logic 1, then the center frequency will be scaled down by 2.5 to 480 Hz. This allows the precision dial tone of 350 Hz/440 Hz to pass, as well as audible ringing at 440 Hz/480 Hz and the busy tone and the precision reorder tone of 480 Hz/620 Hz.

High Band Filter

The high band filter is a 20th order switched capacitor filter consisting of a 10th order bandpass filter and a 10th order allpass filter centered at 2400 Hz. The allpass filter is a delay equalizer that provides compensation for the pass band group delay variation in the high band filter and half of the compromise line characteristics. See Figure 3 for the group delay response of the high band filter and Figure 2 for amplitude response.
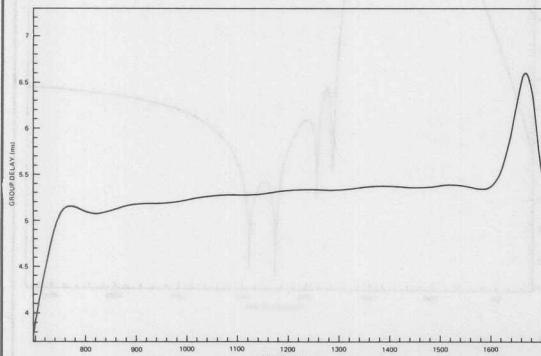
In the Answer mode, the highband filter is used in the transmit path. In the Originate mode, it is used in the receive path.

When analog loop back is used in the Answer mode, the high band filter will be in the test loop. In Call Progress Monitoring mode with SEL 2 (Pin 1) at logic 1 and CPM (Pin 12) at logic 0, the center frequency will be scaled down by a factor of 6 to 400 Hz. If Pin 1 is at logic 0 or Pin 12 is at logic 1 this filter operates in the normal data mode.

In the XR-2129, a 10 dB gain is built into the receive filter path.

Transmit and Receive Output Smoothing Filters

The transmit and receive output smoothing filters are 2nd order, active RC, low pass filters that reconstruct the time sampled output signals characteristic of switched capacitor filters.

V.22 Notch Filter

The V.22 notch filter is a 4th order switched capacitor notch filter cascaded with the low band filter. The notch frequency of the filter is at 550 Hz when NSEL (Pin 17) is logic 0 and is shifted to 1800 Hz when NSEL is logic 1. In the XR-2128 and XR-2129, the notch filter is bypassed in the low band filter if NFI pin is logic 0. On the XR-2126/2127/2128, the notch filter output will always be available at Pin 16 (NFO). On the XR-2129, the NFO pin is not available; the notch filter will appear on Pin 24 (RXC OUT) if (NFI) is logic 1.

Worst Case Line Equalizer

The worst case line equalizer is an optional fixed compromise (amplitude and delay) equalizer designed for worst case line conditions (3002, C_O) in the high band receive mode. The equalizer is inserted in the high band receive path in operating modes 14 and 16 (see Table I).

Uncommitted Operational Amplifiers

Two uncommitted operational amplifiers are provided on all four versions of the modem filters. These are the transmit and receive amplifiers. They can be used as input anti-aliasing filters or as gain stages.


Figure 1. Low Band Group Delay Characteristics
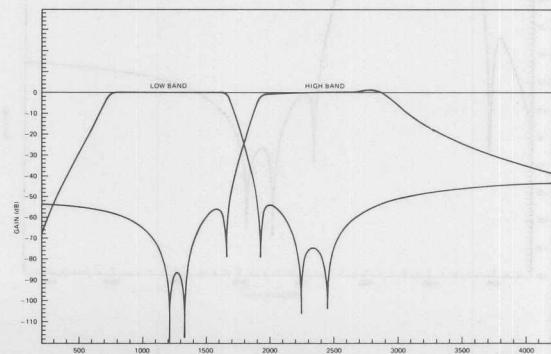
**Figure 2. Low and High Band Amplitude Response**
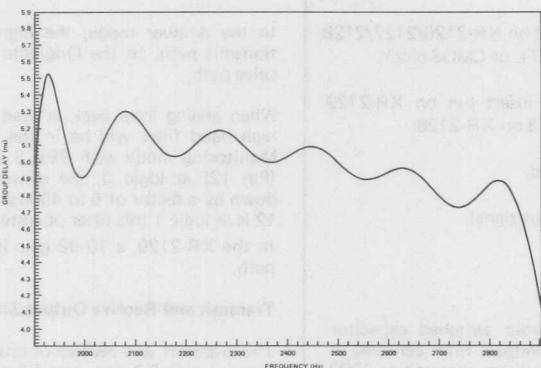
Figure 3. High Band Group Delay Characteristics
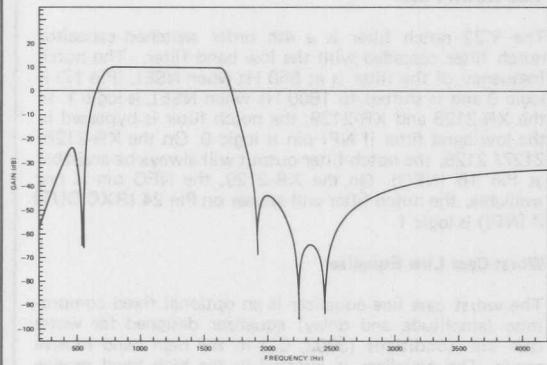

Figure 4A. XR-2129 with 500 Hz Notch
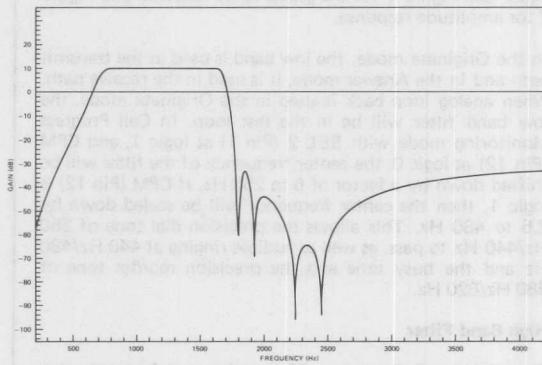

Figure 4B. XR-2129 with 1800 Hz Notch
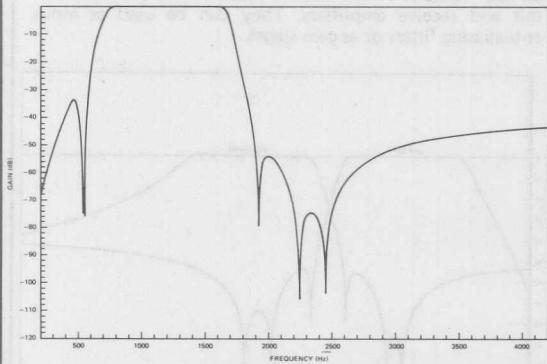
**Figure 5A. XR-2126/2127/2128 with 500 Hz Notch**
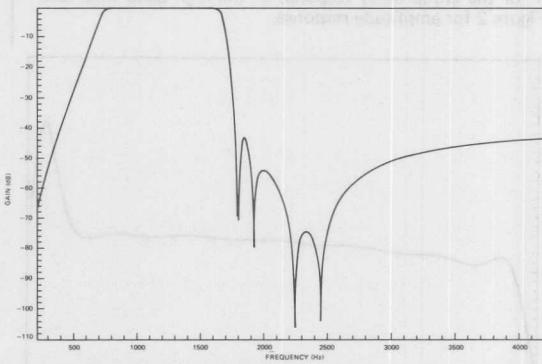
Figure 5B. XR-2126/2127/2128 with 1800 Hz Notch

Analog Loop Back Test

When $\overline{\text{ALB}}$ (Pin 14) on XR-2127, XR-2128 and (Pin 9) on XR-2129 is logic 0, the modem transmit signal, TXC OUT (internally) is looped back to the modem through the RXC OUT pin with no signal present (MUTE) on TXC OUT (output pin). If the low band filter is to be tested, the MODE pin should be logic 0 and logic 1 if the highband filter is to be tested. The receive output smoothing filter will always be in the test loop regardless of the MODE level.

Originate/Answer Mode Selection

When MODE (Pin 11) is logic 0, the modem filter operates in the Originate mode, transmitting in the low band and receiving in the high band. If MODE is logic 1, the modem filter operates in the answer mode; transmitting in the high band and receiving in the low band.

Transmit Squelch in Call Progess Mode

If CPM (Pin 12) is logic 1, the input of the transmit smoothing filter will be disconnected and shorted to ground, muting the transmitter. In the handshake sequence of the Bell 212A modem, this feature can be used to eliminate the transmit signal output.

Phone Line Status Monitor

If the logic levels on the control pins are shown in operation 15 (Table 1), the low band and high band filters will be bypassed; TXC OUT will be connected to TXC IN and RXC OUT will be connected to RXC IN. This feature can be used to monitor the status of the phone line. The output smoothing filters will always be in the TXC OUT and RXC OUT paths.

TABLE I OPERATING MODES

OPERATION	CPM	SEL 2	ALB	MODE	NFI	NSEL	TXC IN	TXC OUT	RXC IN	RXC OUT
0	0	0	1	0	0	X	L	L	H	H
1	0	0	1	1	0	X	H	H	L	L
2	0	0	0	0	0	X	L	MUTE	—	L
3	0	0	0	1	0	X	H	MUTE	—	H
4	0	1	1	0	X	X	L/6	L/6	H/6	H/6
5	0	1	1	1	X	X	H/6	H/6	L/6	L/6
6	0	1	0	0	X	X	L/6	L/6	H/6	L/6
7	0	1	0	1	X	X	H/6	H/6	L/6	H/6
8	1	0	1	0	X	X		MUTE	H	H
9	1	X	1	1	X	X		MUTE	L/2.5	L/2.5
10	1	X	0	0	X	X		MUTE	L/2.5	L/2.5
11	0	1	0	0	X	X		MUTE	—	H
12	0	0	1	0	1	0	H	H	L	L+ 550 Hz Notch
13	0	0	1	0	1	1	H	H	L	L+ 1800 Hz Notch
14	0	0	1	0	1	0	L	L	H	H+ WCL EQ
15	0	0	1	0	1	1	TXC IN	—	RXC IN	
16	0	0	0	0	1	X	H	MUTE	—	H+ WCL EQ
17	0	0	0	0	1	0	L	MUTE	—	L+ 550 Hz Notch
18	0	0	0	0	1	1	L	MUTE	—	L+ 1800 Hz Notch

Note: MUTE means no signal present on transmitter output.
L refers to low band filter with center frequency of 1200 Hz.
H refers to high band filter with center frequency of 2400 Hz.
— means no filter connection.
+ means connection to both filters.
X means "don't care" condition.
N refers to Notch
Mode 15 is filter bypass mode where low band and high band filters are bypassed to monitor status of phone line.
WCL EQ is the Worst Case Line equalizer.

XR-2126/7/8/9
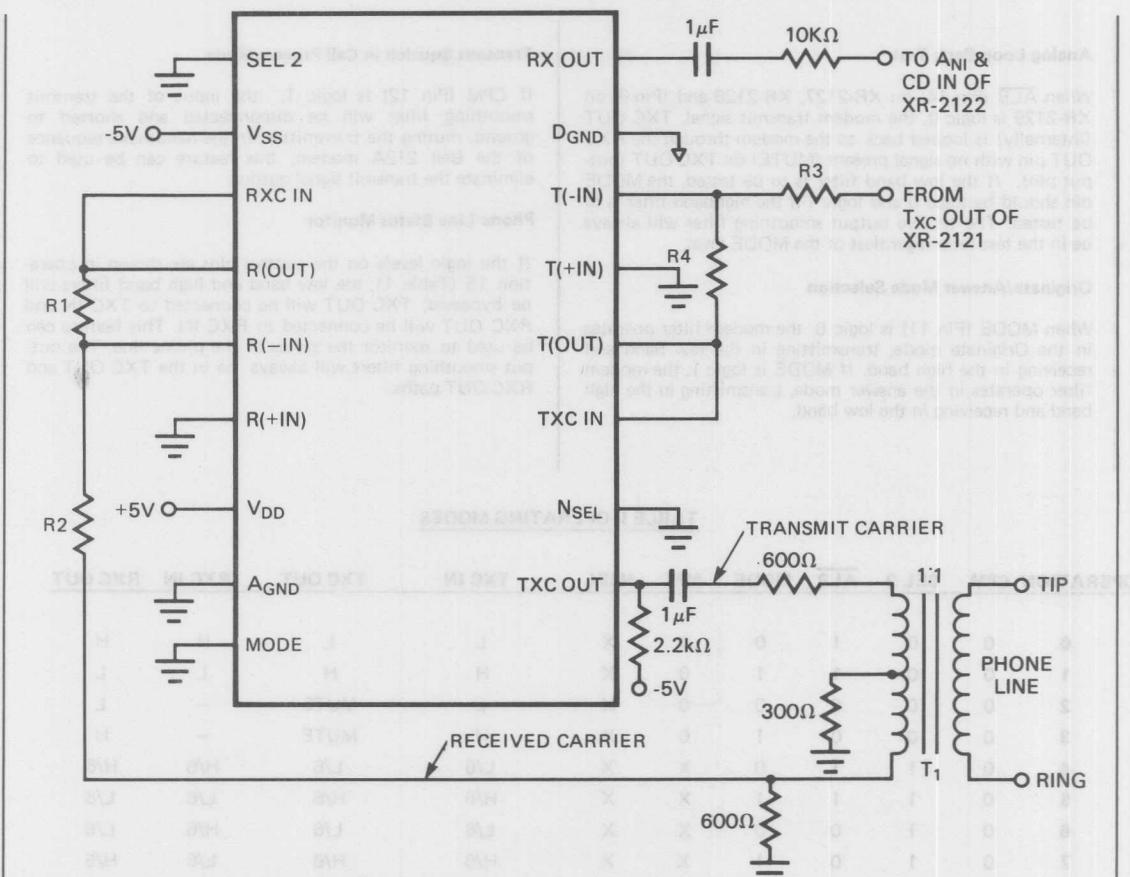
Figure 6. XR-2126/2127/2128/2129 Typical Connection (Spike Supression DAA Not Shown)

Clock Selection (Note 1)

On the XR-2126/2127/2128, SEL 1 (Pin 9) is used to select the internal clock divider (÷8/÷16) depending on the external clock frequency. SEL 1 is set at logic 0 for a 1.2288 MHz input clock and at logic 1 for a 2.4576 MHz clock on CLK 1 (Pin 4). A 153.6 KHz clock input is provided on CLK 2 (Pin 22). If used, CLK 1 (Pin 4) and SEL 1 (Pin 9) should be left open.

On the XR-2129, neither of these clock options are available. Instead, the device operates from an on chip clock oscillator which requires an external 1.8432 MHz crystal. Also available on the XR-2129, is a buffered 1.8432 MHz clock output on Pin 15.

Normal Call Progress/Enhanced Call Progress

When SEL 2 (Pin 1) and CPM (Pin 12) are logic 0, the modem filter operates in the normal modem data mode. If either pin is logic 1, the modem filter operates in the Call Progress Monitoring mode. If SEL 2 is logic 1, and CPM is logic 0, the low band and high band filters will be scaled

down by a factor of 6. If CPM is logic 1, the low band filter will be scaled down by a factor of 2.5 and, depending on the mode on MODE (Pin 11) and ALB (Pin 14), RXC OUT will either be the output of the scaled low band filter (L/2.5) or the unscaled high band filter.

Note 1: When using CLK1, CLK2 may be left open, tied to logic 1, or tied to logic 0. When using CLK2, CLK1 may be floated, tied to logic 1, or tied to logic 0.

TYPICAL APPLICATIONS

XR-2126/2127/2128/2129

The XR-2126 through XR-2129 have a number of common functions. Figure 6 shows typical connection of these functions by their mnemonic. The receive amplifier gain is set by $\dfrac{R1}{R2} = A_{V_{RECEIVED}}$

and transmit amplifier gain is $\dfrac{R4}{R3} = A_{V_{TRANSMIT}}$

SEL 2

SEL 2 (pin 1) allows the sampling clock of the high band filter to be divided down by 6. This reduction of the sampling frequency provides filtering for the Call Progress Monitoring tones. SEL 2 is taken to a logic 1 for Call Progress Monitoring, and is returned to a logic 0 for normal high band filtering. When used in conjunction with the XR-2122 Bell 212A Type Demodulator, Call Progress Tones can be detected by the Energy Carrier Dectect pin of the XR-2122 (pin 17, CD OUT) and the tone identified by its cadence or interruption rate. This is the method used by most Call Progress Decoder ICs. It is assumed that a processor will monitor the Energy Carrier Detect pin of the XR-2122 and a look-up table will be available to match cadence with tone.

DESCRIPTIONS OF INPUTS AND OUTPUTS

VSS

VSS (pin 2) is the negative supply line to the IC. In most modem applications this will be −5 V. A 0.1μF or larger capacitor from this pin to ground is required.

RXC IN

RXC IN (pin 3) is the filter input for the received signal. This signal may be taken directly from the secondary side of the DAA isolation transformer, or may pass through a gain/ anti-aliasing stage.

ROUT, R(−IN), R (+IN)

ROUT (pin 5), R(−IN) (pin 6), and R(+ IN) (pin 7) are respectively the output, inverting input, and non-inverting input of an additional onboard op amp. Figure 3 shows this op amp with gain setting resistors R_1 and R_2. This amplifier may also be used as an anti-aliasing filter. The cut off frequency is chosen to be approximately ¼ of the sampling frequency.

VDD

VDD (pin 8) is the positive supply line to the IC. In most modem applications, this will be 5 V DC. A 0.1μF or larger capacitor from this pin to ground is required.

AGND

AGND (pin 10) is the analog ground line of the IC. It should be connected to all other analog circuitry in a system design.

MODE

MODE (pin 11) sets the mode of operation for the filters. The filters consist of a high band filter with a center frequency at 2400 Hz and a low band filter with a center frequency at 1200 Hz. MODE is used to place the proper filter (2400 Hz or 1200 Hz center frequency) in the proper signal path (transmit or receive). Answer mode MODE logic

1) places the low band filter in the receive path and the high band filter is the transmit path. Originate mode (MODE logic 0) places the high band filter in the receive path and the low band filter in the transmit path.

TXC OUT

TXC OUT (pin 15 for XR-2126/2127/2128 and pin 16 for XR-2129) provides the smoothed transmit signal output. This is typically taken through a 1 μF capacitor and into the secondary of an isolation transformer which represents a 1200Ω load. To drive this load, a 2.2kΩ from TXC output to VSS is needed.

NSEL

NSEL (pin 17) is used to select one of two notch filters which are available for CCITT V.22 mode filtering. A logic 0 on NSEL selects the 550 Hz filter while a logic 1 on NSEL selects the 1800 Hz filter. Both notch filters are in the low band path and are used to attenuate the feedthrough of the transmitted guard tone through the transformer and into the Answer modem's received carrier input to a level much lower than the received carrier. (See Figures 4 and 5.)

TXC IN

TXC IN (pin 18) is the filter input for the transmitted signal.
This signal may be taken directly from TXC ADJ (pin 3) of the XR-2121 Bell 212A Type Modulator.

T(OUT), T(+ IN), T(−IN)

T(OUT) (pin 19), T(+ IN) (pin 20), and T(− IN) (pin 21) are respectively the output, non-inverting input, and inverting input of an additional onboard op amp. Figure 6 shows this op amp with gain setting resistors R_3 and R_4. This op amp may also be used in an anti-aliasing filter. This cut off frequency is chosen to be approximately ¼ of the sampling frequency.

DGND

DGND (pin 23) is the digital ground line of the IC. It should be connected, single point, to all other digital circuitry in a system design.

RXC OUT

RXC OUT (pin 24) provides the smoothed received signal output. This is typically taken through a 1μF capacitor to the AGC circuit and CD IN of the XR-2122 Bell 212A Demodulator.

XR-2126

The XR-2126 has four features in addition to those common to the other members of this filter family. They are CLK 1, SEL 1, NFO, and CLK 2.

XR-2126/7/8/9

CLK 1

CLK 1 (pin 4) is one of two clock inputs for the XR-2126. Either clock input may be used (CLK 1 or CLK 2). CLK 1 will accept either a 2.4576 MHz input or a 1.2288 MHz input, depending on the state (logic 1 or logic 0 respectively) of SEL 1.

SEL 1

SEL 1 (pin 9) selects either the 2.4576 MHz clock or the 1.2288 MHz clock for input on pin 4, CLK 1.

NFO

NFO (pin 16) is the notch filter output.

CLK 2

CLK 2 (pin 22) takes a 153.6 KHz TTL or CMOS clock input.

XR-2127

The XR-2127 has five functions in addition to those common to the other members of this filter family. They are CLK 1, SEL 1, ALB, NFO, and CLK 2.

CLK 1

CLK 1 (pin 4) is one of two clock inputs for the XR-2127. Either clock input may be used (CLK 1 or CLK 2). CLK 1 will accept either a 2.4576 MHz input or a 1.2288 MHz input, depending on the state (logic 1 or logic 0 respectively) of SEL 1.

SEL 1

SEL 1 (pin 9) selects either the 2.4576 MHz clock or the 1.2288 MHz clock for input on pin 4, CLK 1.

$\overline{ALB}$

$\overline{ALB}$ (pin 14) selects the Analog Loop Back mode when logic 0. A logic 1 on $\overline{ALB}$ allows normal operation.

NFO

NFO (pin 16) is the notch filter output.

CLK 2

CLK 2 (pin 22) takes a 153.6 KHz TTL or CMOS clock input.

XR-2128

The XR-2128 has seven functions in addition to those common to the other members of this filter family. They are CLK 1, SEL 1, CPM, NFI, ALB, NFO, CLK 2.

CLK 1

CLK 1 (pin 4) is one of two clock inputs for the XR-2128. Either clock input may be used (CLK 1 or CLK 2) CLK 1 will accpet either a 2.4576 MHz input or a 1.2288 MHz input, depending on the state (high or low respectively) of SEL 1.

SEL 1

SEL 1 (pin 9) selects either the 2.4576 MHz clock or the 1.2288 MHz clock for input on pin 4, CLK 1.

CPM

CPM (pin 12) selects normal low band filter operation and divides by 2.5 for Call Progress Monitoring use. Logic is TTL with a logic 0 for normal low band operation and a logic 1 for low band divided by 2.5 for enhanced Call Progress Monitoring.

NFI

NFI (pin 13) selects the low band filter path. With NFI logic 1, the notch filter (550 Hz or 1800 Hz) selected by NSEL (pin 17) is inserted in the low band filter signal path. With NFI logic 0, the signal bypasses the notch filters.

$\overline{ALB}$

$\overline{ALB}$ (pin 14) selects the Analog Loop Back mode when logic 0. A high on $\overline{ALB}$ allows normal operation.

NFO

NFO (pin 16) is the notch filter output.

CLK 2

CLK 2 (pin 22) takes a 153.6 KHz TTL or CMOS clock.

XR-2129

The XR-2129 is designed specifically for use with the XR-212AS chip set (XR-2125, XR-2121, and XR-2122 excluding the XR-2120). This part requires no division of the 1.8432 MHz clock oscillator frequency. A 1.8432 MHz crystal is connected between XTAL IN and XTAL OUT (pins 13 and 14 respectively). Figure 7 shows the XR-212AS chip set using the XR-2129 in place of the XR-2120 to complete the Bell 212A Modem Signal Processor.

The XR-2129 has six functions in addition to those common to the other members of this filter family. They are $\overline{ALB}$, CPM, XTAL IN, XTAL OUT, CLK OUT, NFI.

$\overline{ALB}$

$\overline{ALB}$ (pin 9) selects the Analog Loop Back mode when logic 0. A logic 1 on $\overline{ALB}$ allows normal operation.

CPM

CPM (pin 12) is used to select either normal low band operation (fo = 1200 Hz) or low band divided by 2.5 (fo = 480 Hz). Logic is TTL with a logic 0 for normal low band operation and a logic 1 for low band divided by 2.5 for Call Progress Monitoring.

XTAL IN, XTAL OUT

XTAL IN (pin 13) and XTAL OUT (pin 14) are the oscillator nodes across which a 1.8432 MHz crystal must be connected for operation. This 1.8432 MHz crystal is the same frequency crystal required for operation of the XR-2121, XR-2122, and XR-2125. The buffered output from this onboard oscillator is available from CLK OUT (pin 15). XTAL OUT (pin 14) offers the unbuffered oscillator output.

CLK OUT

CLK OUT (pin 15) provides the buffered output from the onboard oscillator. It can be used to drive other circuitry requiring a 1.8432 MHz clock.

NFI

NFI (pin 22) selects the low band filter path. With NFI logic 1, the notch filter (550 Hz or 1800 Hz) selected by NSEL (pin 17), is inserted in the low band filter signal path. With NFI logic 0, the notch filters are bypassed by the signal.

XR-2126/7/8/9

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RS232 CONNECTOR

XR-2121
1	A GND	D GND	22
2	V_SS	EXT T_XCLK	21
3	T_XC ADJ	NC	20
4	T_XC OUT	CLK IN	19
5	T_XC EN	DIB CLK	18
6	1200/300	NC	17
7	V_DD	MODE	16
8	NC	T_XD	15
9	T_XCLK	NC	14
10	NC	SCR EN	13
11	NC	NC	12

XR-2125
1	SB	V_DD	14
2	T_XEN	T_XD OUT	13
3	R_XEN	T_XCLK IN	12
4	T_XDIN	CLK IN	11
5	R_XD OUT	R_XD IN	10
6	R_XCLK OUT	R_XCLK IN	9
7	V_SS	10/9	8

XR-2129
1	SEL 2	R_X OUT	24
2	V_SS	D_GND	23
3	R_XC IN	NFI	22
4	NC	T(-IN)	21
5	R(OUT)	T(+IN)	20
6	R(-IN)	T(OUT)	19
7	R(+IN)	T_XC IN	18
8	V_DD	NSEL	17
9	ALB	T_XC OUT	16
10	A_GND	CLK OUT	15
11	MODE	XTAL OUT	14
12	CPM	XTAL IN	13

XR-2122
1	A_NI	V_DD	28
2	A_INV	F_ADJ	27
3	A_OUT	CSH	26
4	DEMOD IN	RT	25
5	RCV OUT	CT	24
6	CD IN	CT	23
7	A GND	EYE	22
8	NC	D GND	21
9	CLK IN	R_XDNS	20
10	1200/300	R_XD	19
11	MODE	R_XCLK	18
12	HS	CD	17
13	C_DELAY	PSK CD	16
14	V_SS	FSK CD	15

1.8432 MHz

2.2kΩ

5.1V

1:1:1

PHONE LINE

R_1	200K	R_9	1K	*TXC Amplifier Adjust
R_2	50K	R_{10}	1M	
R_3	100K	R_{11}	511K	
R_4	100K	R_{12}	1K	C_1	1μF	C_4	1μF
R_5	600	R_{13}	100K	C_2	0.001μF	C_5	1μF
R_6	300	R_{14}	10K	C_3	.0033μF	C_6	0.47μF
R_7	600	R_{15}	390K			C_7	1μF
R_8	200K			T_1	MIDCOM 671-0313

Q_1 | 2N4961

IC1 | XR-1489 | Resistors -10%
IC2 | XR-1488 | Capacitors -20%
IC3 | CD-4069

Figure 7. XR-212AS Bell 212A Modem Utilizing the XR-2129 Modem Filter

XR-212AS Modem System

INTRODUCTION

This application note describes a four-chip modem set designed to perform the complete Bell 212A type modem function. Described are the functions of each device, the connection of the four together, and testing procedures with performance data.

PRINCIPLES OF OPERATION

The basic characteristics of the 212A type modem are listed in Figure 1. As seen, this type of system is basically a dual modem. It can communicate with either low speed FSK modems (Bell 100 Series) or at 1200 BPS to PSK modems.

Figure 2 illustrates the major components of most modem systems. The four sections are:

1. **Modem Signal Processor (MSP):** This is the heart of the modem. It contains the modulator, demodulator, and filtering functions.

2. **Data Coupler:** This section in the 212A is a direct access arraignment (DAA). This type is directly connected to the switched telephone network. The DAA serves to protect the phone network from modem and vice versa.

3. **UART:** Performs serial to parallel conversion and timing functions.

4. **Handshaking Controls:** Timing functions for signals such as clear to send (CTS) and request to send (RTS).

The XR-212A consists of the following four devices which perform the complete MSP function.

XR-2120 PSK Modem Filter: This is a switched capacitor type filter for providing precise filtering and equalization for both 300 BPS FSK and 1200 BPS PSK carrier signals.

XR-2121 - PSK/FSK Modulator: Complete modulation functions are performed by this device for both 300 BPS FSK and 1200 BPS PSK.

XR-2122 - PSK/FSK Demodulator: Demodulation of FSK or PSK encoded carriers is performed by the XR-2122.

XR-2125 - Data Buffer: Performs asynchronous to synchronous and synchronous to asynchronous conversion.

```
MAJOR 212A TECHNICAL SPECIFICATIONS

DATA RATES:
    Low Speed Mode:
        0-300 BPS Asynchronous Format
    High Speed Mode:
        1200 BPS Character-Asynchronous Format
        1200 BPS Synchronous Format

ENCODING FORMATS:
    Low Speed Mode:
        FSK (Frequency Shift Keying)
    High Speed Mode:
        PSK (Phase Shift Keying)

OPERATING MODE:
    Full-Duplex at all Speeds

LINE REQUIREMENT:
    Two-Wire Switched Network
```

Figure 1. Major 212A Technical Specifications
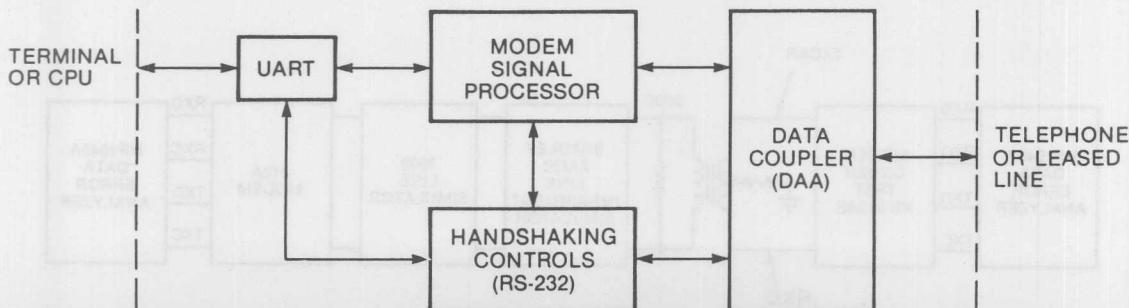
Figure 2. Modem Architecture

AN-28

COMPLETE SYSTEM

Figure 3 is a simplified schematic intended to illustrate the complexity of the system.

Figure 5 illustrates the complete schematic diagram of the XR-212AS.

A performance test set-up is illustrated in Figure 4 The data error analyzers send a known data pattern and analyze whether this data was correctly received and demodulated. These analyzers give a quantitative number for errors received. On the line side of the modems there is a line simulator to introduce amplitude and group delay characteristics to the transmission channel as in an actual phone line. Most testing would include performance data for three different lines, C2 - nominal or normal line, C0 (3002) - worst case line, and back-to-back - no line. The XR-212AS is optimized for C2 line conditions (fixed compromise equalization in the XR-2120, however, it is important to know per-

formance over other line conditions which may occur in an actual telephone link. The last piece in the test set-up is the line impairment simulator which can add impairments to the carrier signal which may exsist in the telephone channel. These impairments include noise and frequency offset.

The major specification often used to judge a modem's quality is its bit error rate (BER) as a function of interfering noise or signal to noise ratio (S/N).

Figures 6, 7, and 8 illustrate the typical BER vs. S/N performance for the XR-212AS operating at 1200 BPS for the three different line conditions. The data taken for these figures is under the following conditions:

$$R_{XC} = -40 \text{ dBM}$$
$$T_{XC} = -10 \text{ dBM}$$
511 Random Data Pattern
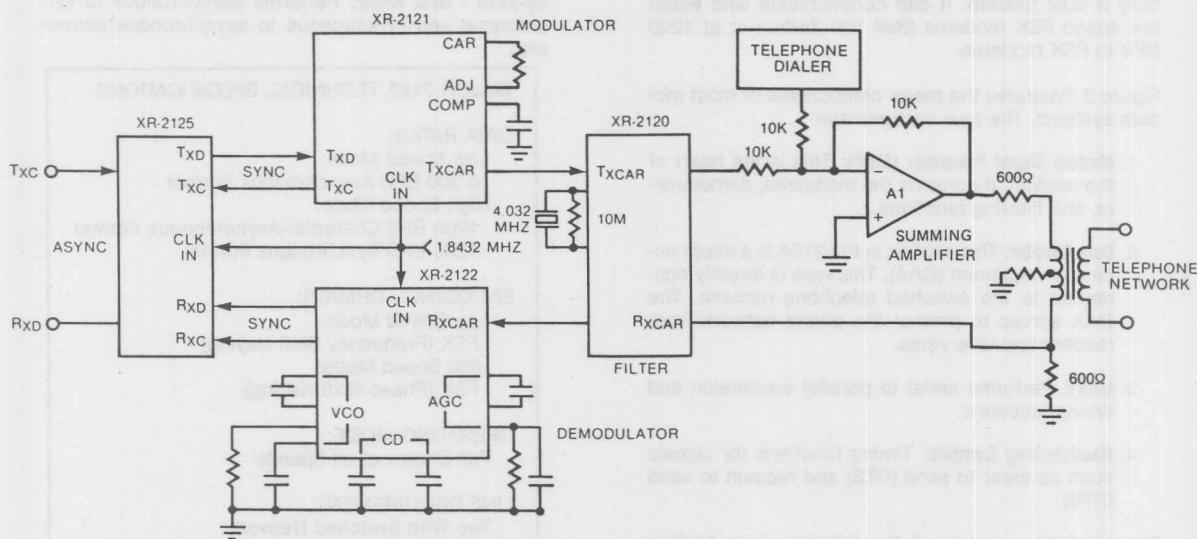
Figure 3. Complete Modem Signal Processor
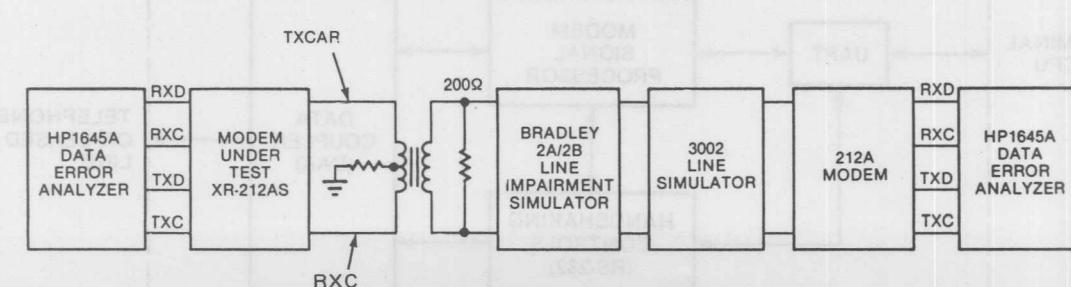

Figure 4. Performance Test Set-Up
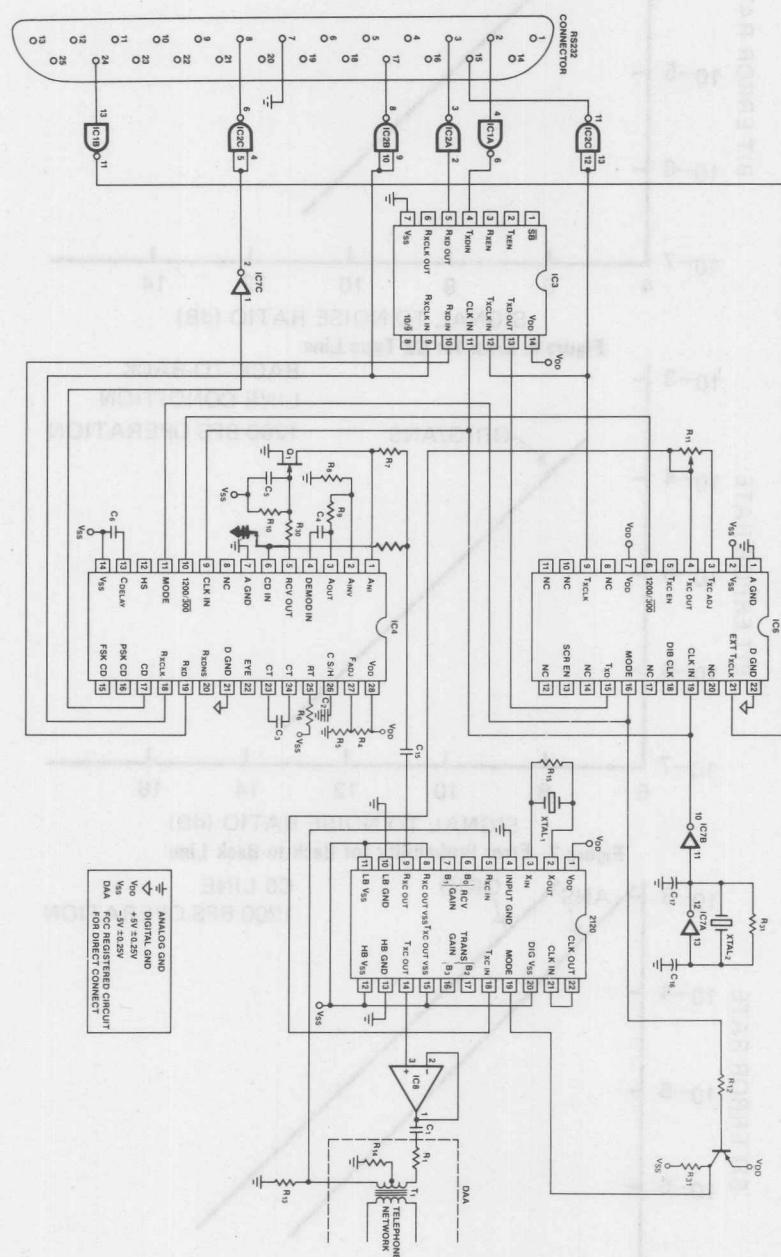
Figure 5. Complete 212AS Schematic

**C2 LINE
ANSWER OR
ORIGINATE MODE
1200 BPS OPERATION**
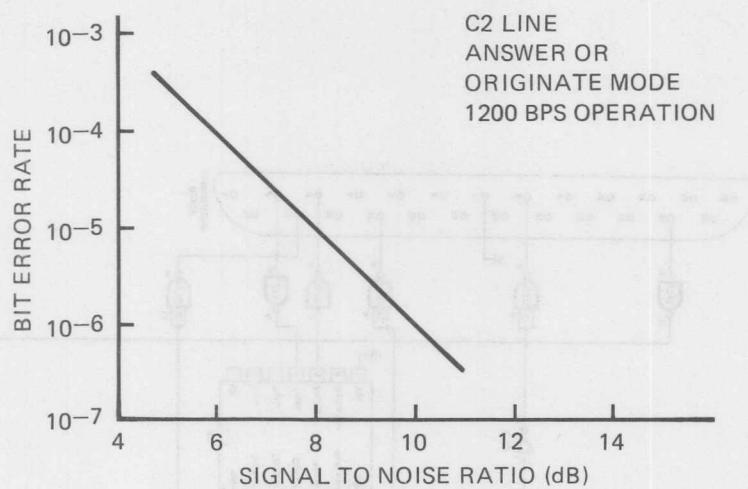
Figure 6. Error for C2 Type Line

**BACK-TO-BACK
LINE CONDITION
1200 BPS OPERATION**

ORIG/ANS
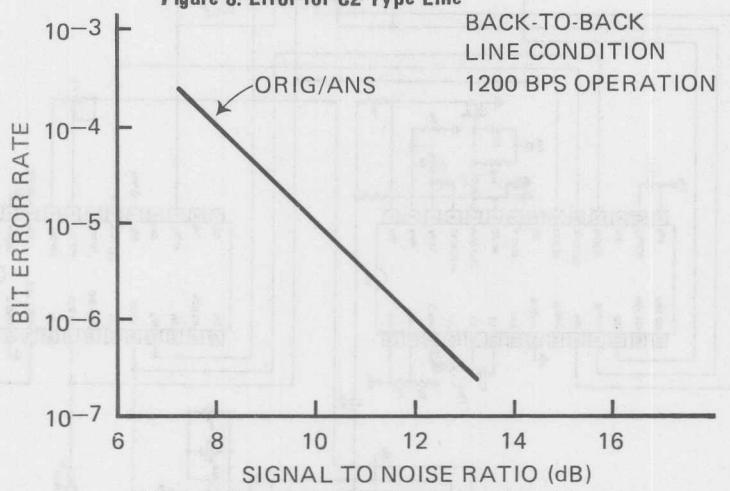
Figure 7. Error Probability for Back-to-Back Line

ANS   ORIG

**C0 LINE
1200 BPS OPERATION**
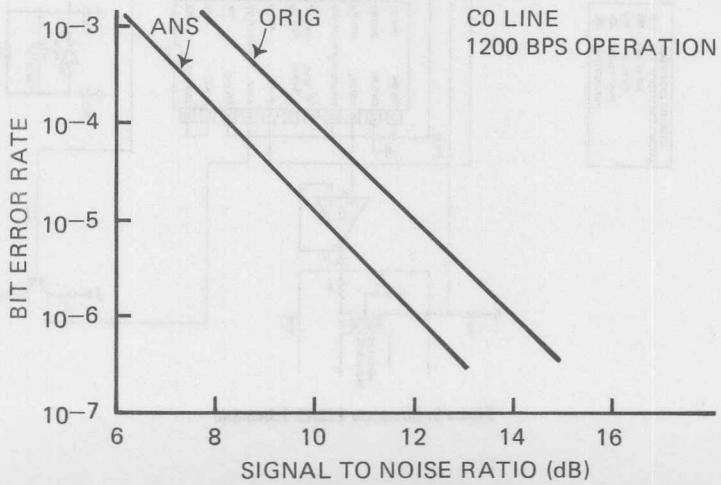
Figure 8. Error Probability for C0 Type Line

XR-212AS Parts List

R1	600
R4	200K 1%
R5	1K 1%
R6	390K
R7	33K
R8	1K
R9	100K
R10	1M
R11	10K Potentiometer
R13	600
R14	300
R15	10M
R16 - R29	20K
R30	511K
R31	10M

C1	$1\mu f$
C2	$0.01\mu f$
C3	$.0033\mu f$
C4 - C5	$1\mu f$
C6 - C14	$.47\mu f$
C15	$1\mu f$
C16	10pf
C17	10pf

CRYSTALS

XTAL 1 - 4.032 MHz M-TRON
XTAL 2 - 1.8432 MHz X-TRON

TRANSFORMER

T1 - 671-1066 MIDOM or 671-0313 MIDCOM

FET

2N4861

IC1	XR-1489
IC2	XR-1488
IC3	XR-2125
IC4	XR-2122
IC5	XR-2120
IC6	XR-2121
IC7	CD4069
IC8	XR-1458

APPENDIX G
Bell Dial-up Line Characteristics

BELL SCHEDULE	3002	C1	C2	C4	DCS-S#
Attenuation Characteristic (referenced to 1000 Hz)	300 to 3000 Hz −3 to +12 dB	300 to 2700 Hz −2 to +6 dB	300 to 3000 Hz −2 to +6 dB	300 to 3200 Hz −2 to +6 dB	300 to 3000 Hz −1 to +3 dB
Envelope Delay Distortion (max. μsec)	800 to 2600 Hz 1750 μsec	1000 to 2400 Hz 1000 μsec	1000 to 2600 Hz 500 μsec	1000 to 2600 Hz 300 μsec	1000 to 2600 Hz 100 μsec
		800 to 2600 Hz 1750 μsec	600 to 2600 Hz 1500 μsec	800 to 2800 Hz 500 μsec	600 to 2600 Hz 300 μsec
			500 to 2800 Hz 3000 μsec	600 to 3000 Hz 1500 μsec	500 to 2800 Hz 600 μsec
				500 to 3000 Hz 3000 μsec	

APPENDIX H
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-- NOTES --